# MB65
# TFT IDTV
## SERVICE MANUAL

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# INTRODUCTION

17MB65 main board is driven by MStar SOC. This IC is capable of handling Video and audio processing, Scaling-Display processing, 3D comb filter, OSD and text processing, LVDS transmitting, channel and MPEG2/4 decoding, integrated DVB-T/C demodulator and media center functionality.

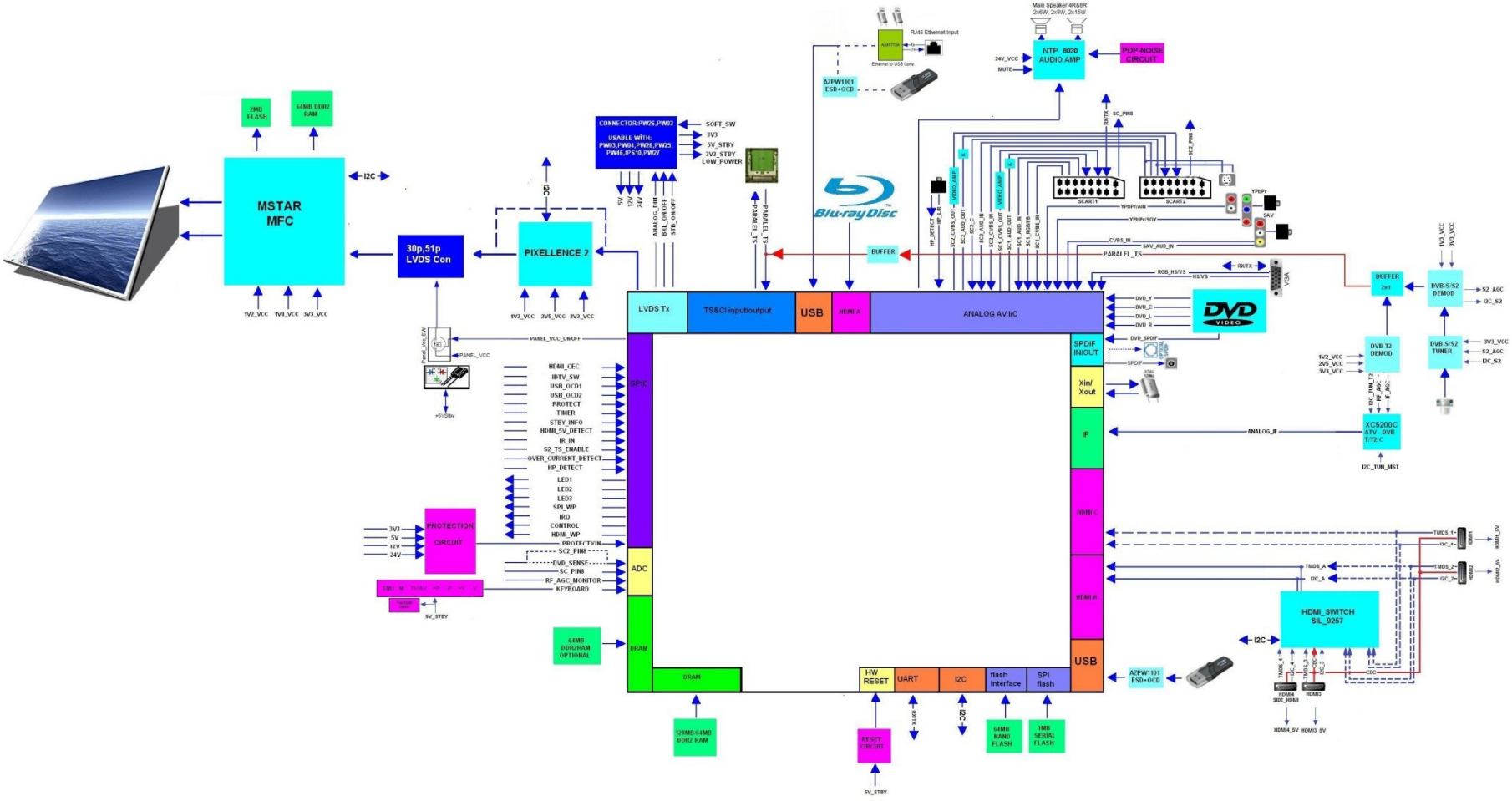
TV supports PAL, SECAM, NTSC color standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo. Also DVB T, DVB-C are supported internal demodulators of Mstar IC and DVB-T2 is supported with external demodulator.

Sound system output is supplying max. 2x8W (1%THD) for stereo 8Ω speakers

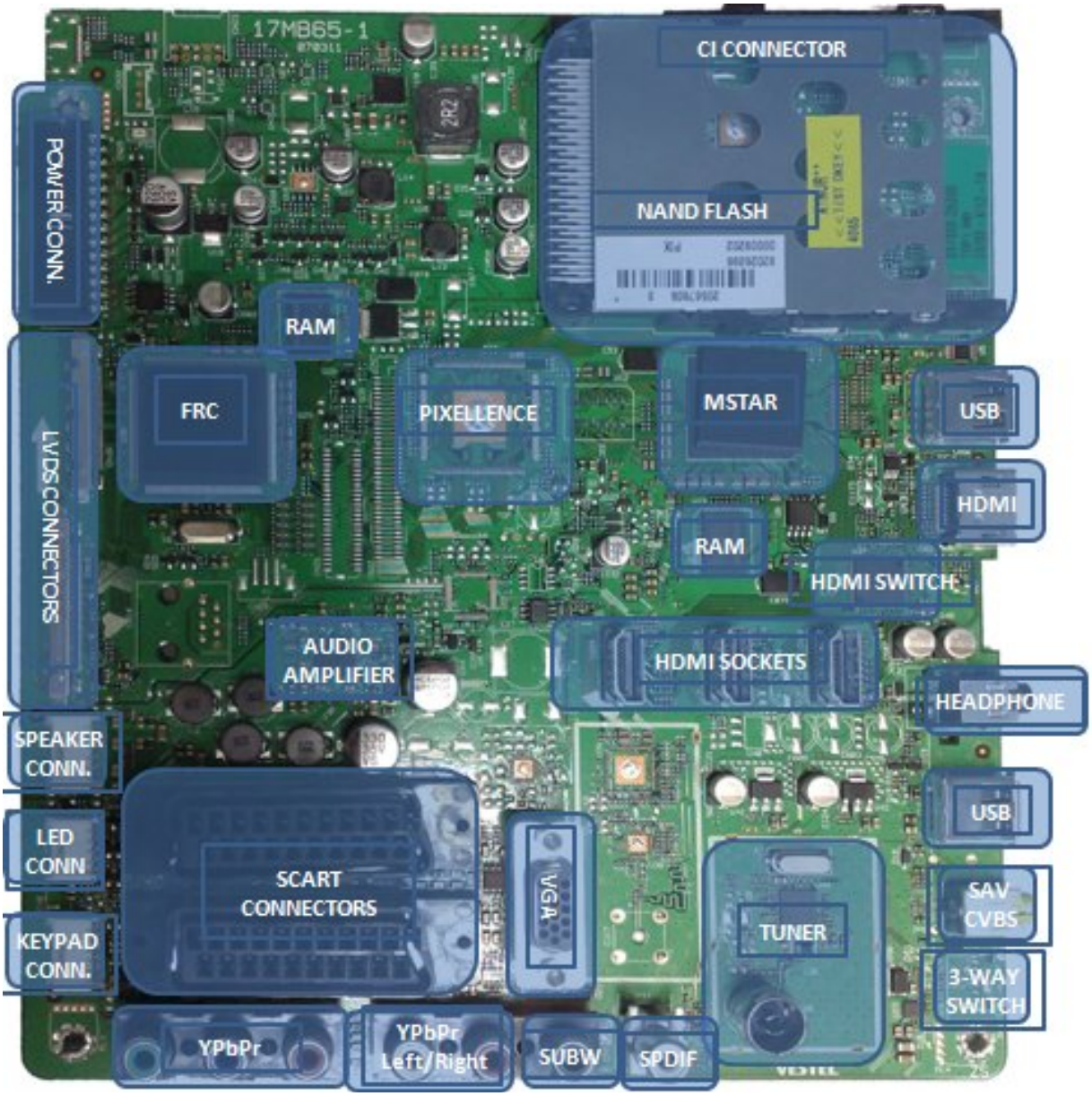
Supported peripherals are:

1 RF input VHF I, VHF III, UHF @ 75Ohm(Common)
1 Side AV (CVBS, R/L_Audio)
2 SCART socket(Common)
1 YPbPr (Common)
1 PC input(Common)
4 HDMI 1.3 input(2 HDMI inputs are common, 4 inputs are optional)
1 S/PDIF output(Common)
1 Headphone(Common)
1 Common interface(Common)
2 USB(Common)
1 DVD(Optional)
1 External Keypad(Optional)
1 External TouchPad(Optional)

## General Block Diagram



## MB65 Placement of Blocks



# 1. TUNER(XC5200)

The Single-Chip Multi-Standard Tuner XC5200C supports all analog TV formats transmitted worldwide in the 42-1000 MHz band on either cable or terrestrial broadcast channels. It implements on-chip tuning, and channel filtering without external (SAW) filters and has no manually tunable parts.

The broadband tuner converts the selected channel into an Intermediate Frequency (IF), which is then sampled by an internal high-resolution analog-to-digital converter (A/D) for further processing..

The IF signals are filtered using a standard-dependent high-rejection channel filter and converted to a user-programmable output frequency. At the output of the D/A converter, the TV signal is low-pass filtered using a high-performance smoothing filter and input to a variable gain amplifier. The IF output amplifier gain can be controlled via an external analog signal on Vagc.

## 1.1. General description of Samsung XC5200:

Tuner XC5200C supports all analog TV formats transmitted worldwide in the 42-1000 MHz band on either cable or terrestrial broadcast channels and the broadband tuner converts the selected channel into an Intermediate Frequency (IF).

## 1.2. Features:

- Receiving System: All analog TV formats transmitted worldwide in the 42-1000 MHz band on either cable or terrestrial broadcast channels
- Highly integrated tuner design (no SAWs):
  Alignment-free
  Quartz-stable and accurate
  No externally tunable parts
- Multi-standard RF-to-IF receiver
- Integrated RF PLL filter reducing risk of noise pickup on the board
- Integrated DSP for high quality IF filtering both in analog and digital modes
- ATV mode optimized for use with external analog demodulators
- DTV Mode for operation with external DTV demodulator. XC5200C applies filters and converts signal to arbitrary output frequency. Supports standards such as ATSC, OpenCable, DVB-C, DVB-T, ISDB-T, DMB-TH

## 1.3. Pinning:

| # | Name | Type | Description |
|---|---|---|---|
| B | GNDA | S | Main analog ground |
| 1 | VDDA | S | 3.3V supply |
| 2 | IN1 | RF/I | RF input 1; connected to GND through 390nH inductor. |
| 3 | GND | S | Ground |
| 4 | IN2 | RF/I | RF input 2 (as secondary input for FM radio. Connect to ground if unused) |
| 5 | GND | S | Ground |
| 6 | ExtChoke | RF | External low-VHF choke inductor. 820nH against VDDA |
| 7 | GND | S | Ground |
| 8 | VDDA | S | 3.3V supply |
| 9 | VDDA | S | 3.3V supply |
| 10 | NC | | Not connected internally |
| 11 | NC | | Not connected internally |
| 12 | VDDC | S | 1.8V supply (mixed-signal) |
| 13 | VDDC | S | 1.8V supply (mixed-signal) |
| 14 | VDDA | S | 3.3V supply (main analog) |
| 15 | Vagc | A/I | Control voltage for output IF signals. ( AGC for digital reception only) |
| 16 | DIFP | A/O | Positive IF signal to digital demodulator |
| 17 | VDDA | S | 3.3V supply |
| 18 | DIFN | A/O | Negative IF signal to digital demodulator |
| 19 | GND | S | Ground |
| 20 | VDDC | S | 1.8V supply (mixed-signal) |
| 21 | VDDA | S | 3.3V supply |
| 22 | GND | S | Ground |
| 23 | GPIO_3 | D/IO | General purpose input/output |
| 24 | TestMode | D/I | Used for production tests only. (do not connect) |
| 25 | GPIO_2 | D/IO | General purpose input/output |
| 26 | VDDC | S | 1.8V supply (Mixed-signal) |
| 27 | GPIO_1 | D/IO | General purpose input/output |
| 28 | AddrSel | A/I | Select $I^2C$ address; internal 1MΩ pull-down. Selection among 4 addresses if the pin is externally set at 0; VDDA/3;2VDDA/3;VDDA |
| 29 | X2 | A | External crystal |
| 30 | GND | A | Ground |
| 31 | X1 | A | External crystal |
| 32 | ExtRef | D/I | Ext. ref. frequency (1.8V or 3.3V; internal pull-down). Supersedes internal oscillator if a valid clock signal is provided. Do not connect for typical applications, if internal crystal oscillator is used. |
| 33 | VDDD | S | 1.8V supply (DSP-digital) |
| 34 | SCL | D/I | $I^2C$ SCL signal (clock) |
| 35 | SDA | D/IO | $I^2C$ SDA signal (data) |
| 36 | GND | S | Ground |
| 37 | Reset | D/I | Reset; active low; pull-up (3.3V). In test mode: select operation<br>1mS Reset duration is recommended after power-on |
| 38 | VDDA | S | 3.3V |
| 39 | NC | | Not connected internally |
| 40 | V120 | A | Output of on-chip voltage regulator, 1.2V, connect capacitor to GND |
| 41 | V145 | A | Output of on-chip voltage regulator, 1.45V, connect capacitor to GND |

## 1.4. IF Filter Responses:

DTV6 - 6MHz Channel Bandwidth:

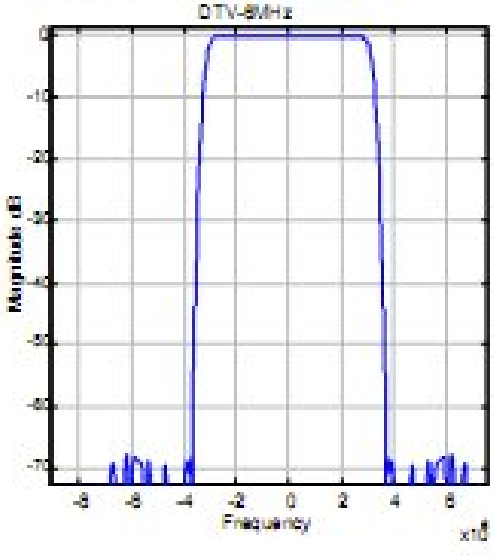



Figure 2. DTV6 response shown to -70 dB

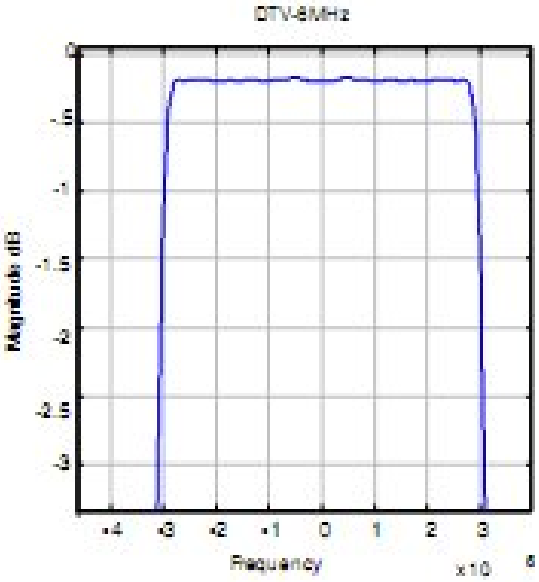



Figure 3. DTV6 response shown to -3 dB

DTV8 - 8MHz Channel Bandwidth:

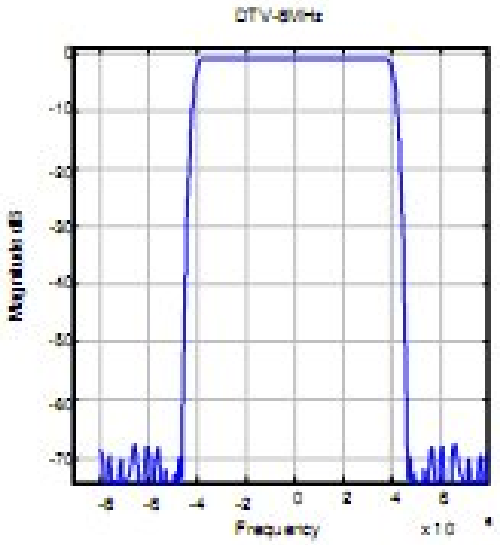



Figure 4. DTV8 response shown to –70 dB

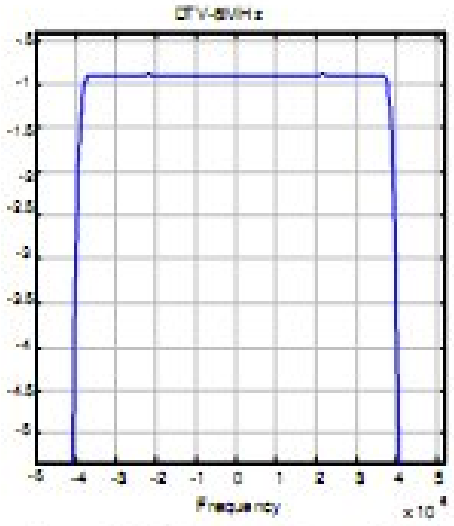



Figure 5. DTV8 response shown to -3 dB

# 2. AUDIO AMPLIFIER STAGE WITH NTP8030(U21)

## 2.1. General Description

The NTP-8030 is a single chip full digital audio amplifier including power stage for stereo amplifier system. NTP-8030 is integrated with versatile digital audio signal processing functions, high-performance, high-fidelity fully digital PWM modulator and two high-power full bridge MOSFET power stages. The NTP-8030 receives digital serial audio data with sampling frequency from 8KHz to 192KHz. It delivers 2 x 30 watt in stereo mode without heat sink. The NTP-8030 has mixer and Bi-Quad filters which can be used to implement the essential audio signal processing functions like loudness control, loud speaker response compensation and parametric equalizers. All the functions of the NTP-8030 can be controlled by internal register values via I2C host interface bus.

## 2.2. Features

- 2 CH Stereo (30W x 2 BTL)
- Wide Operating Supply Voltage Range (7.5V to 30V)
- Floating Point Operation
- 16 Programmable Bi-Quad Filters
- Speaker Compensation
- DC Cut, LPF, HPF
- Parametric Equalizer
- 100dB Dynamic Range
- Enhanced Dynamic Range Control
- Adaptive Loudness Compensation
- Loudness Control
- Protection Circuit
- OCP(Over Current Protection)
- OTP(Over Temperature Protection)
- UVP(Under Voltage Protection)
- High Efficiency

## 2.3. Absolute Ratings

### 2.3.1. Electrical Characteristics

#### 2.3.1.1. Absolute Maximum Ratings

| Parameter | Reference | Rating | Unit |
|---|---|---|---|
| DVDD voltage | DVSS | -0.3 ~ 2.5 | V |
| VDD_IO voltage | VSS_IO | -0.3 ~ 4.4 | V |
| Logic input voltage | VSS_IO | -0.3 ~ 5.5 | V |
| Logic output voltage | VSS_IO | -0.3 ~ 4.4 | V |
| PVDDXX voltage | PGNDXX | 32 | V |
| OUTXX voltage | PGNDXX | -0.3 ~ PVDDXX | V |
| BSTXX voltage | PGNDXX | 47 | V |
| VDRXX voltage | PGNDXX | 15 | V |
| Storage Temperature | Tstg | -55 ~ 150 | °C |
| Junction Temperature | Tj | 150 | °C |

#### 2.3.1.2. Recommended Operating Conditions

| Parameter | Reference | Rating | Unit |
|---|---|---|---|
| DVDD voltage | DVSS | 1.82 ~ 1.98 | V |
| VDD_IO voltage | VSS_IO | 3.0 ~ 3.6 | V |
| PVDDXX voltage | PGNDXX | 7.5 ~ 30 | V |
| VDRXX voltage | PGNDXX | 8~14 | V |
| Ambient Operating temperature | Tamb | -10 ~ 85 | °C |

### 2.3.1.3. Electrical Characteristics

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Logic Block** (DVDD=1.8V, VDD_IO=3.3V, $T_A$=+25°C, unless otherwise specified.) | | | | | | |
| Input High Voltage | $V_{ih}$ | - | 2.0 | | | V |
| Input Low Voltage | $V_{il}$ | - | -0.3 | | 0.8 | V |
| Threshold point | $V_t$ | - | | 1.09 | | V |
| Schmitt trig. Low to High threshold point | $V_{t+}$ | - | 1.4 | | 2.0 | V |
| Schmitt trig. High to Low threshold point | $V_{t-}$ | - | 0.8 | | 1.2 | V |
| Input Current | $I_i$ | VDD_IO=MAX, 0V ≤ Vin ≤ 5.5V | | | ±10 | uA |
| | | 40kΩ pull down | 40 | | 180 | uA |
| | | 40k Ω pull up | -180 | | -40 | uA |
| Output Low Voltage | $V_{ol}$ | $I_{ol}$=2,4,...24mA | | | 0.4 | V |
| Output High Voltage | $V_{oh}$ | $I_{oh}$=-2,-4,...-24mA | 2.4 | | | V |
| Output Low Current | $I_{ol}$ | $V_{ol}$=0.4V, 4mA | 4.7 | 8.0 | 10 | mA |
| Output High Current | $I_{oh}$ | $V_{oh}$=2.4V, 4mA | 5.8 | 11.9 | 19 | mA |
| **Driver Block** (PVDDXX=20V, $T_A$=+25°C, unless otherwise specified.) | | | | | | |
| OUT On Resistance | $R_{dson}$ | PVDDXX=7.5V | | 0.165 | | Ω |
| Peak Current Limit | OCP | - | 3.75 | 5 | | A |
| Thermal Shutdown Temperature | | | | 150 | | °C |

### 2.3.1.4. Performance Specifications

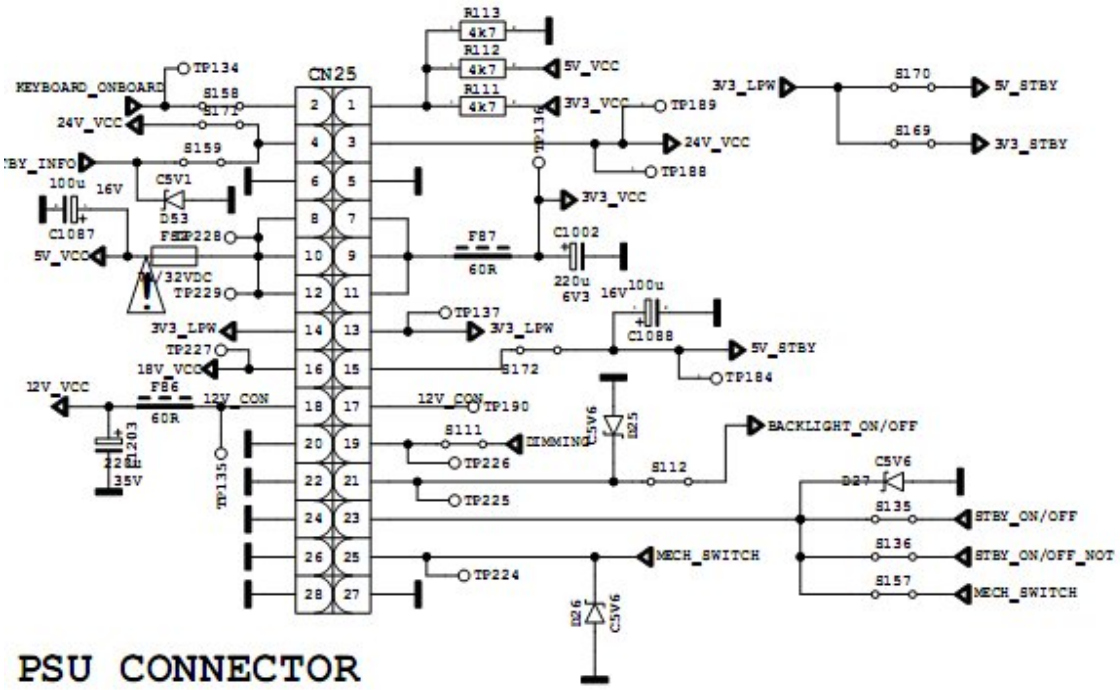
| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SNR | AES17, A-weighting filter | | 100 | | dB |
| THD+N | 1W, 1kHz | | 0.01 | | % |
| Cross talk | Dolby standard | | 70 | | dB |
| PSRR | $V_{RIPPLE}$=1Vrms, Audio Input= -60dBFS | | 88 | | dB |
| Power consumption | PVDD=24V, Output Power=10W@8Ω | | TBD | | W |
| Peak Output Power | PVDD=27V @8Ω | | 30 | | W |

## 2.4. Pinning

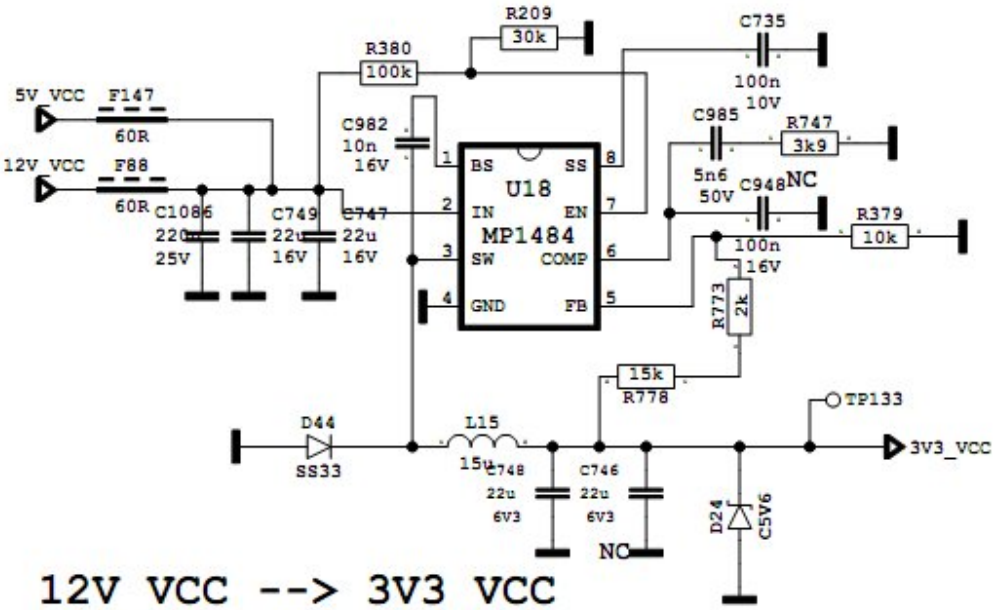
| PIN | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | BST1A | P | Bootstrap supply, external capacitor to OUT1A is required |
| 2 | VDR1A | P | Gate drive voltage regulator decoupling pin, capacitor to GND is required |
| 3 | /RESET | I | Active low to reset NTP-8030, Schmitt trigger input |
| 4 | AD | I | I2C device address selection |
| 5 | DGND | P | Ground for Core block |
| 6 | GND_IO | P | Ground for digital interface I/O |
| 7 | CLK_I | I | System master clock, Schmitt trigger input |
| 8 | VDD_IO | P | Power supply for digital interface I/O, 3.3V |
| 9 | DGND_PLL | P | Ground for PLL digital block |
| 10 | AGND_PLL | P | Ground for PLL analog block |
| 11 | LF | O | External PLL loop filter |
| 12 | AVDD_PLL | P | Power supply for PLL analog block, 1.8V |
| 13 | DVDD_PLL | P | Power supply for PLL digital block, 1.8V |
| 14 | GND | I | This pin should be connected to Ground |
| 15 | DGND | P | Ground for Core block |
| 16 | DVDD | P | Core Logic Power Supply, 1.8V |
| 17 | SDATA | I | I2S serial data input |
| 18 | WCK | I/O | I2S word clock |
| 19 | BCK | I/O | I2S bit clock |
| 20 | SDA | I/O | I2C data |
| 21 | SCL | I | I2C clock |
| 22 | MONITOR0 | O | No Connection, monitoring signal out from Power Driver protection logic |
| 23 | MONITOR1 | O | No Connection, monitoring signal out from processor block |
| 24 | MONITOR2 | O | No Connection, monitoring signal out from processor block |
| 25 | /FAULT | I | Active low to reset internal power stage, Pull-up |
| 26 | VDR2B | P | Gate drive voltage regulator decoupling pin, capacitor to GND is required |
| 27 | BST2B | P | Bootstrap supply, external capacitor to OUT2B is required |
| 28 | PGND2B | P | Ground |
| 29 | PGND2B | P | Ground |
| 30 | OUT2B | O | Power stage PWM output 2B |
| 31 | OUT2B | O | Power stage PWM output 2B |
| 32 | PVDD2B | P | Power supply for PWM Power stage 2B |
| 33 | PVDD2B | P | Power supply for PWM Power stage 2B |
| 34 | PVDD2A | P | Power supply for PWM Power stage 2A |
| 35 | PVDD2A | P | Power supply for PWM Power stage 2A |
| 36 | OUT2A | O | Power stage PWM output 2A |
| 37 | OUT2A | O | Power stage PWM output 2A |
| 38 | PGND2A | P | Ground |
| 39 | PGND2A | P | Ground |
| 40 | BST2A | P | Bootstrap supply, external capacitor to OUT2A is required |
| 41 | VDR2A | P | Gate drive voltage regulator decoupling pin, capacitor to GND is required |
| 42 | NC | - | No Connection |

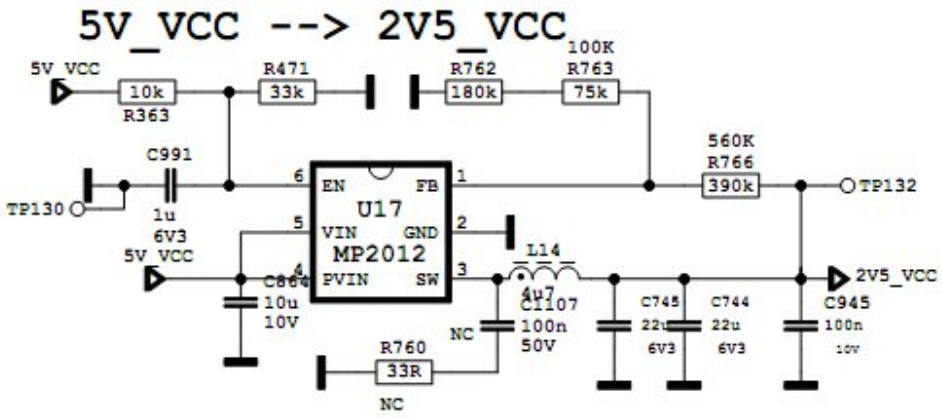
# 3. POWER STAGE

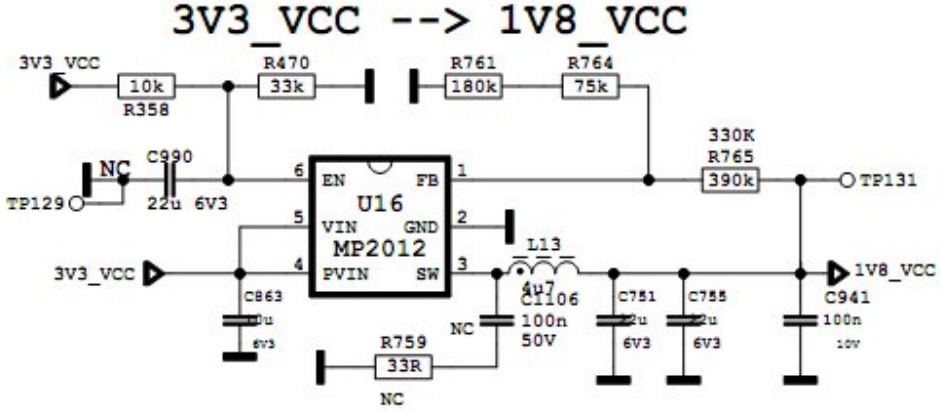
The DC voltages required at various parts of the chassis and panel are provided by a main power supply unit. MB65 chassis can operate with PW03, PW04, PW06, PW07, PW25, PW26, PW27, PW46 as main power supply



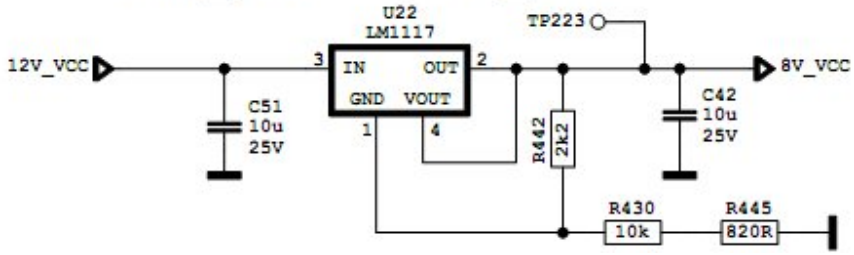

The power supplies generate 18V, 12V, 5V, 3,3V DC voltages. Power stage which is on-chassis generates 1V2, 2V5, 1V8, 8V and 3V3 for PW06 and PW25. These are indicated below.

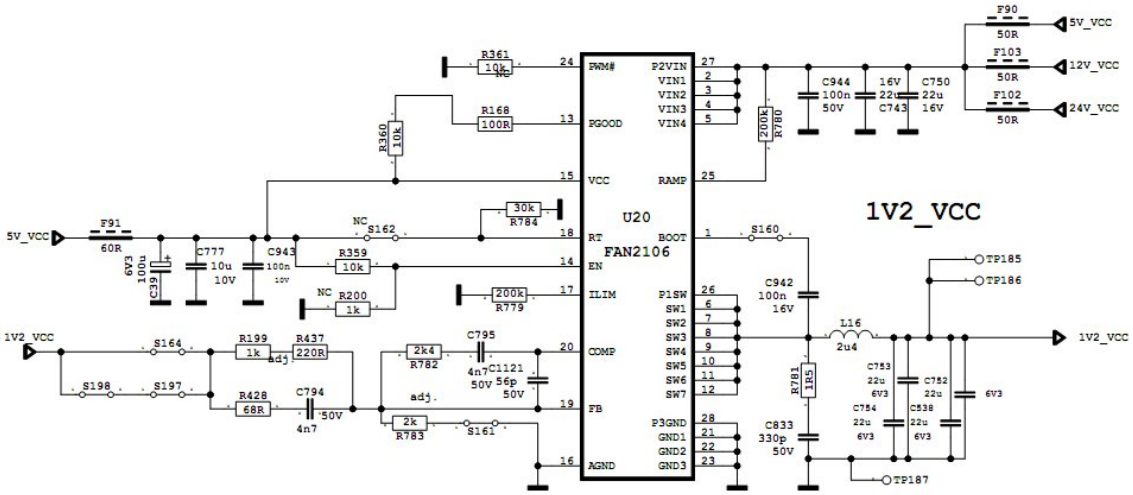

R209
30k
C735
100n
10V
R380
100k
5V_VCC
F147
60R
12V_VCC
F88
60R
C982
10n
16V
C985
5n6
50V
R747
3k9
C948
NC
R379
10k
C1086
22u
25V
C749
22u
16V
C747
22u
16V
U18
MP1484
BS
SS
IN
EN
SW
COMP
GND
FB
100n
16V
R773
2k
15k
R778
TP133
D44
SS33
L15
15u
C748
22u
6V3
C746
22u
6V3
NC
D24
C5V6
3V3_VCC
12V_VCC --> 3V3_VCC


5V_VCC --> 2V5_VCC
5V_VCC
10k
R363
R471
33k
R762
180k
100K
R763
75k
560K
R766
390k
TP132
C991
1u
6V3
TP130
5V_VCC
U17
MP2012
EN
FB
VIN
GND
PVIN
SW
L14
4u7
C1107
100n
50V
NC
C745
22u
6V3
C744
22u
6V3
C945
100n
2V5_VCC
C864
10u
10V
R760
33R
NC

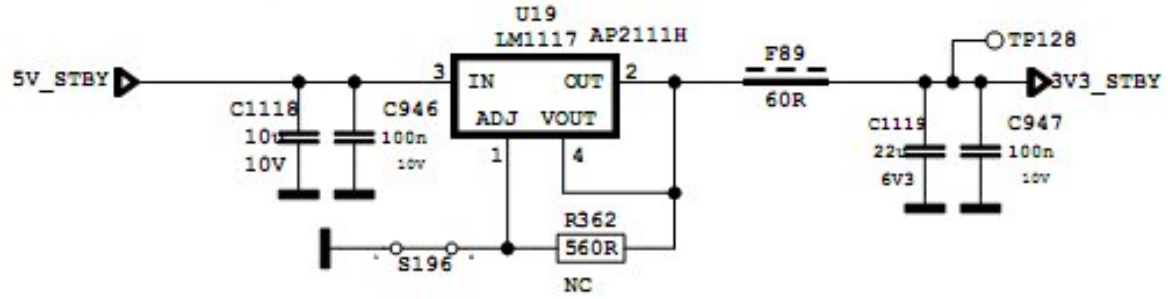

3V3_VCC --> 1V8_VCC
3V3_VCC
10k
R358
R470
33k
R761
180k
R764
75k
330K
R765
390k
TP131
NC
C990
22u
6V3
TP129
U16
MP2012
EN
FB
VIN
GND
PVIN
SW
L13
4u7
C1106
100n
50V
NC
C751
C755
C941
100n
1V8_VCC
C863
R759
33R
NC

# 12V_VCC --> 8V_VCC



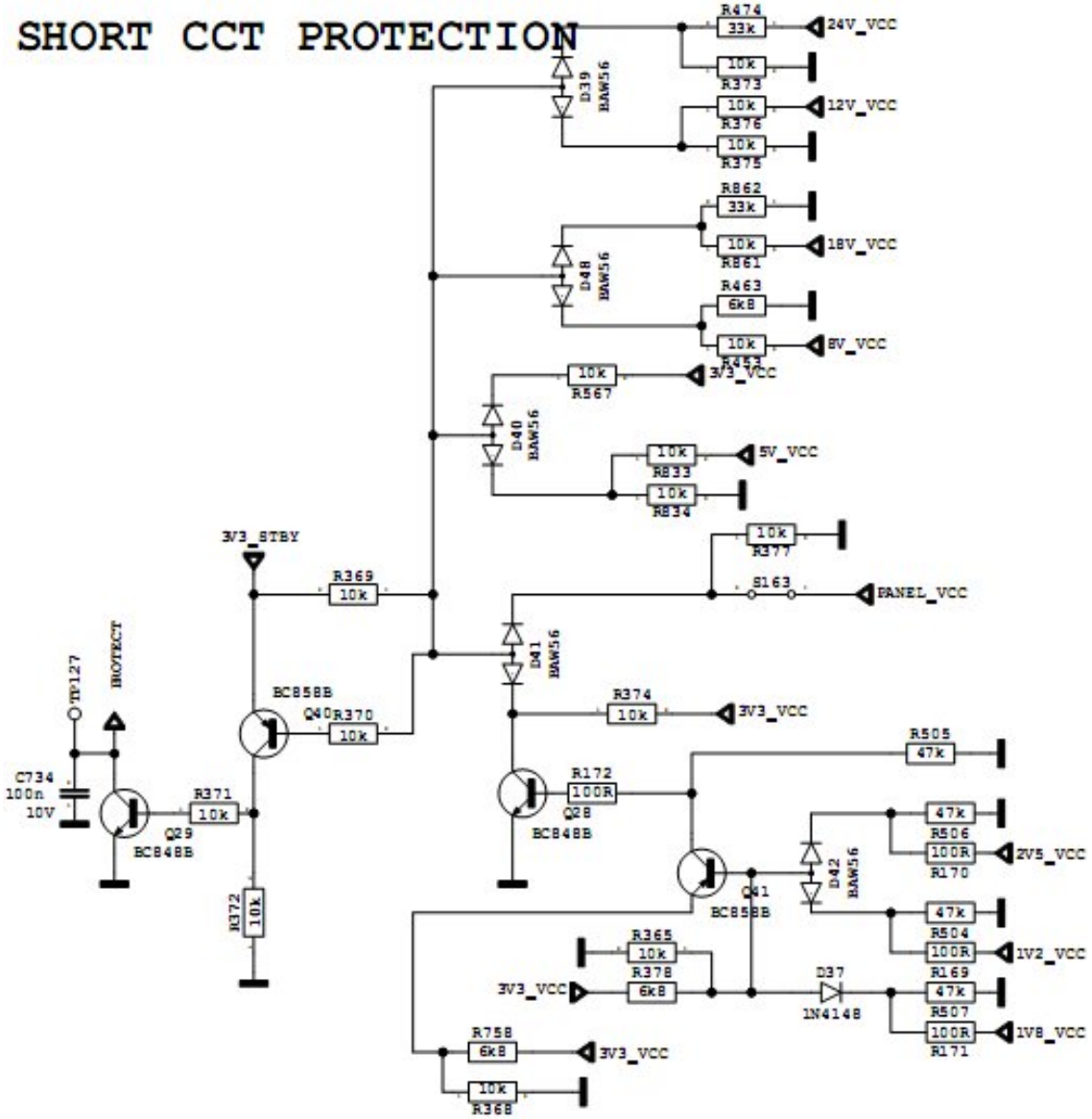




# 4V2_STBY / 5V_STBY--> 3V3_STBY



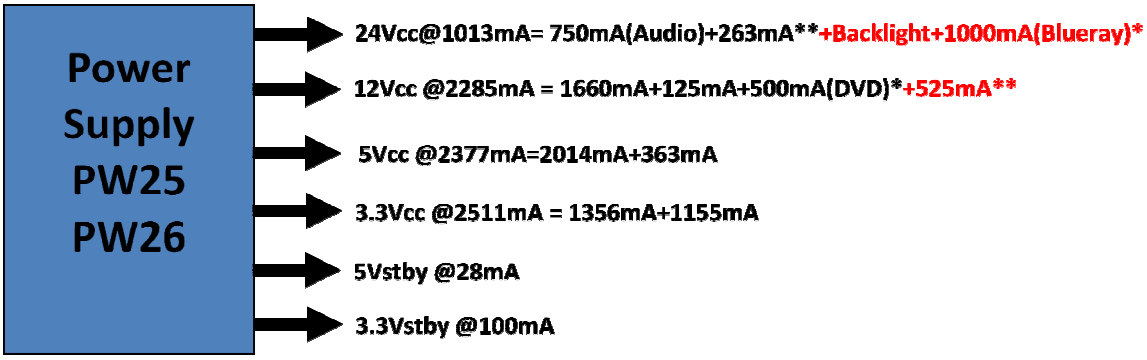
**Short CCT Protection Circuit**

Short circuit protection is necessary for protecting chassis and main IC against damages when any Vcc supply shorts to ground. Protect pin should be logic high while normal operation. When there is a short circuit protect pin should be logic low. After any short detection, SW forces LEDs on LED card to blink.



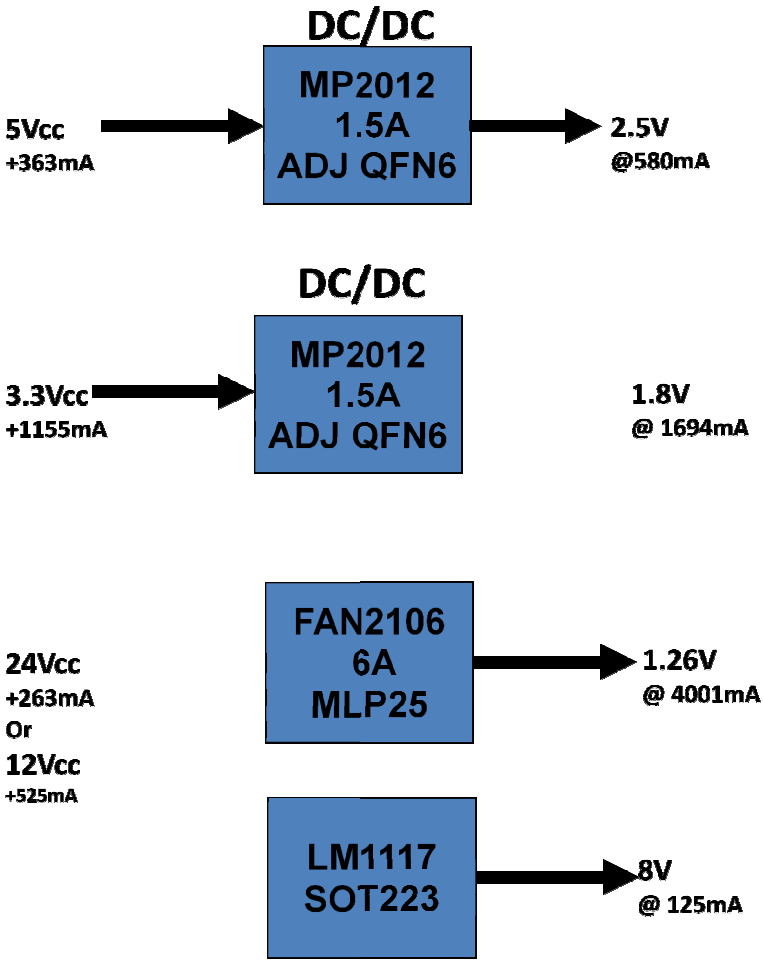
## 3.1. Power Management

### 3.1.1. MB65 Power Management W/PW26




* Optional DVD 12V(500mA) / Blueray 24V(1000)

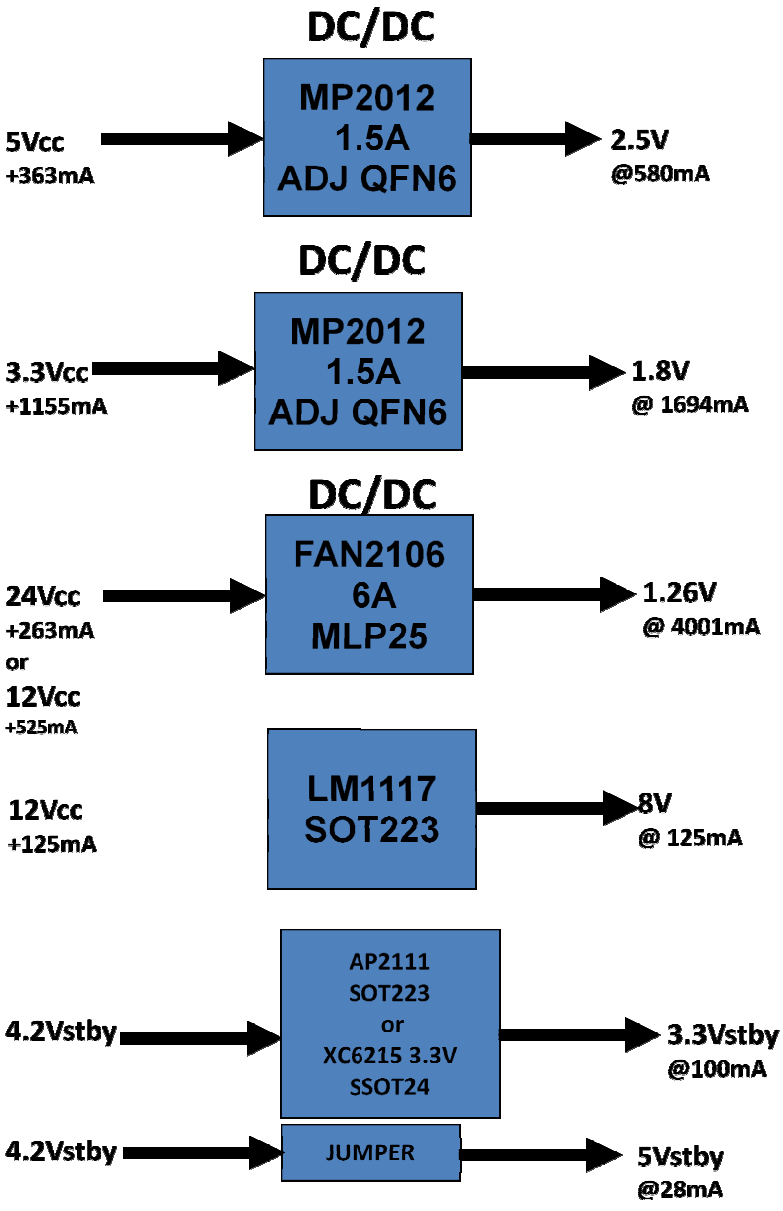
* *1.26V DC/DC Input Optional 12V(525mA)/24V(263mA)



### 3.1.2. MB65 Power Management W/PW25& PW27& PW46 & PW03 & PW04


* Optional DVD 12V(500mA) / Blueray 24V(1000)

* * 1.26V DC/DC Input Optional 12V(525mA)/24V(263mA)



# 4. MICROCONTROLLER – MSTAR(U7)

## 4.1. General Description

The MSD9WB7PX-2 integrates DTV/multi-media all-purpose AV decoder, DVB-T demodulator, VIF demodulator, and Sound/Video processor into a single device. This allows the overall BOM to be reduced significantly making the MSD9WB7PX-2 a very competitive multi-media DTV solution. For ATV users, the MSD9WB7PX-2 provides multi-standard analog TV support with adaptive 3D video decoding and VBI data extraction. The build-in audio decoder is capable of decoding FM, AM, NICAM, A2, BTSC and EIA-J sound standards. The MSD9WB7PX-2 supplies all the necessary A/V inputs and outputs to complete a receiver design including a multi-port HDMI receiver and component video ADC. All input selection multiplexed for video and audio are integrated, including full SCART support with CVBS output. The equipped MStar MACE-5 color engine is the latest masterpiece from MStar famous color engine series providing excellent video and picture quality in Full-HD and large-scale displaying system. To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MSD9WB7PX-2 has an ultra low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

## 4.2. General Features

MSD9WB9PX-2, an SOC solution that supports channel decoding, MPEG decoding, and media-centre functionality enabled by a high performance AV CODEC and CPU Key features include,

- Digital and Analog DVB Front-End Demodulator
- A Multi-Standard A/V Format Decoder
- The MACE-5 Video Processor
- Home Theater Sound Processor
- Peripheral and Power Management

**Transport Stream De-multiplexer**

- Supports parallel and serial TS interface, with or without sync signal
- Supports TS input and output for external CI module
- Maximum TS data rate is 104 Mb/sec for serial or 16 MB/sec for parallel
- 32 general purpose PID filters and section filters for each transport stream de-multiplexer
- Supports additional audio/video/PCR filters
- Supports TS DMA channel for time-shift
- Supports 3DES/DES and AES encryption/decryption

**MPEG-2 Video Decoder**

- ISO/IEC 13818-2 MPEG-2 video MP@HL
- Automatic frame rate conversion
- Supports resolution up to HDTV (1080i, 720p) and SDTV

**MPEG-4 Video Decoder**

- ISO/IEC 14496-2 MPEG-4 ASP video decoding
- Supports resolutions up to HDTV (1080p@30fps)
- Supports DivX1 Home Theater & HD profilesOptional
- Supports VC-1Optional, FLV video format decoding

**H.264 Decoder**

- ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 4.1) video decoding
- Supports resolutions for all DVB, ATSC, HDTV, DVD and VCD
- Supports resolution up to 1080p@30fps
- Supports CABAC and CAVLC stream types
- Processing of ES and PES streams, extraction and provision of time stamps
- Up to 40 Mbits bitrate (Blu-ray spec.)

**Hardware JPEG**

- Supports sequential mode, single scan
- Supports both color and grayscale pictures
- Following the file header scan the hardware decoder fully handles the decode process
- Supports programmable Region of Interest (ROI)
- Supports formats: 422/411/420/444/422T
- Supports scaling down ratios: 1/2, 1/4, 1/8
- Supports picture rotation

**NTSC/PAL/SECAM Video Decoder**

- Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
- Automatic standard detection
- Motion adaptive 3D comb filter
- Five configurable CVBS & Y/C S-video inputs
- Supports Teletext, Closed Caption (analog CC 608/ analog CC 708/digital CC 608/digital CC 708), V-chip and SCTE

**Multi-Standard TV Sound Processor**

- SIF audio decoding
- Supports BTSC/A2/EIA-J demodulation
- Supports NICAM/FM/AM demodulation
- Supports MTS Mode Mono/Stereo/SAP in BTSC/EIA-J mode
- Supports Mono/Stereo/Dual in A2/NICAM mode
- Built-in audio sampling rate conversion (SRC)
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
- Advanced sound processing options available, for example: Dolby, SRS, BBE, QSound, Audyssey
- Supports digital audio format decoding:
- MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3), AAC-LC
- Supports Optional Dolby Digital Plus, Dolby Pulse, and MS10 multi stream decoder, including Dolby Digital Encoder for transcoding streams to Dolby Digital 5.1 (DDCO)
- Supports MPEG Audio, Dolby Digital, Dolby Digital Plus format AD (Audio Description)
- Supports PVR and time-shifting

**Audio Interface**

One SIF audio input interface with minimal external saw filters

- Four L/R audio line-inputs including Mic. input
- Two L/R outputs for main speakers and additional line-outputs
- Supports stereo headphone driver
- I2S digital audio input & output
- S/PDIF digital audio output
- HDMI audio channel processing
- Programmable delay for audio/video synchronization

**Analog RGB Compliant Input Port**

- Three analog ports support up to 1080P
- Supports PC RGB input up to SXGA@75Hz
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG Sync-on-Green
- Automatic color calibration
- AV-link support

**Analogue RGB Auto-Configuration & Detection**

- Auto input signal format and mode detection
- Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
- Sync Detection for H/V Sync

**DVI/HDCP/HDMI Compliant Input Port**

- Three HDMI/DVI Input ports
- HDMI 1.3 Compliant
- HDCP 1.1 Compliant
- 225MHz @ 1080P 60Hz input with 12-bit Deep-color support
- CEC support
- Single link DVI 1.0 compliant
- Robust receiver with excellent long-cable support

**MStar Advanced Color Engine (MStarACE-5)**

- 10/12-bit internal data processing
- Fully programmable multi-function scaling engine
- Nonlinear video scaling supports various modes including Panorama
- Supports dynamic scaling for VC-1
- High-Quality DTV video processor
- 3D motion video deinterlacer with motion object stabilizer
- Edge-oriented deinterlacer with edge and artifact smoother
- Automatic 3:2/2:2/M:N pull-down detection and recovery
- 3D multi-purpose noise reduction for DTV or lousy air/cable input
- MPEG artifact removal including de-blocking and mosquito noise reduction
- Arbitrary frame rate conversion
- MStar Professional Picture Enhancement:
    - Dynamic brilliant and fresh color
    - Dynamic *Blue Stretch*
    - Intensified contrast and details
    - Dynamic *Vivid Skin*
    - Dynamic sharpened Luma/Chroma edges
    - Global and local dynamic depth of field perception
    - Accurate and independent color control
    - Supports sRGB and xvYCC color processing
    - Supports HDMI 1.3 deep color format
- Programmable 12-bit RGB gamma CLUT

**Output Interface**

- Single/dual link 8/10-bit LVDS output
- Supports panel resolution up to Full-HD (1920x1080) @ 60Hz
- Supports TH/TI format
- Supports dithering options to 6/8-bit output
- Spread spectrum output for EMI suppression

**CVBS Video Encoder**

- Supports all NTSC/PAL TV Standard
- Stand-alone scaling engine
- Programmable Hue, Contract, Brightness
- Supports TTX/CC/WSS output

**CVBS Video Output**

- Allows CVBS output of all source inputs

**2D Graphics Engine**

- Hardware Graphics Engine for responsive interactive applications
- Supports point draw, line draw, rectangle draw/fill, text draw and trapezoid draw
- BitBlt, stretch BitBlt, trapezoid BitBlt, mirror BitBlt and rotate BitBlt
- Raster Operation (ROP)
- Support Porter-Duff

**VIF Demodulator**

- Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards
- Audio/Video dual-path processor
- Stepped-gain PGA with 25 dB tuning range and 1 dB tuning resolution
- Maximum IF gain of 37 dB
- Programmable TOP to accommodate different tuner gain and SAW filter insertion loss to optimize noise and linearity performance
- Multi-standard processing with single SAW
- Supports silicon tuner low IF output architecture

**DVB-T/DVB-C Demodulator**

- Digital carrier frequency offset correction: ±500KHz
- Optimized for SFN channels with pre/post-cursive echoes inside/outside the guard
- Acquisition range ±857kHz includes up to 3x: ±1/6 MHz transmitter offset
- Meets Nordig Unified 1.0.3, D-Book 5.0, EICTA E-Book/C-Book test requirement
- ITU J.83 Annex A/C, DVB-C (EN 300 429) compliant
- Supports DVB-C 0.7-7M Baud symbol rate
- ±400kHz internal carrier offset recovery range
- 6.8 usecs echo cancellation at 7 Msym/s
- Supports IF, low-IF, zero-IF inputs
- Ultra-fast automatic blind UHF/VHF channel scan (constellations and symbol rate)

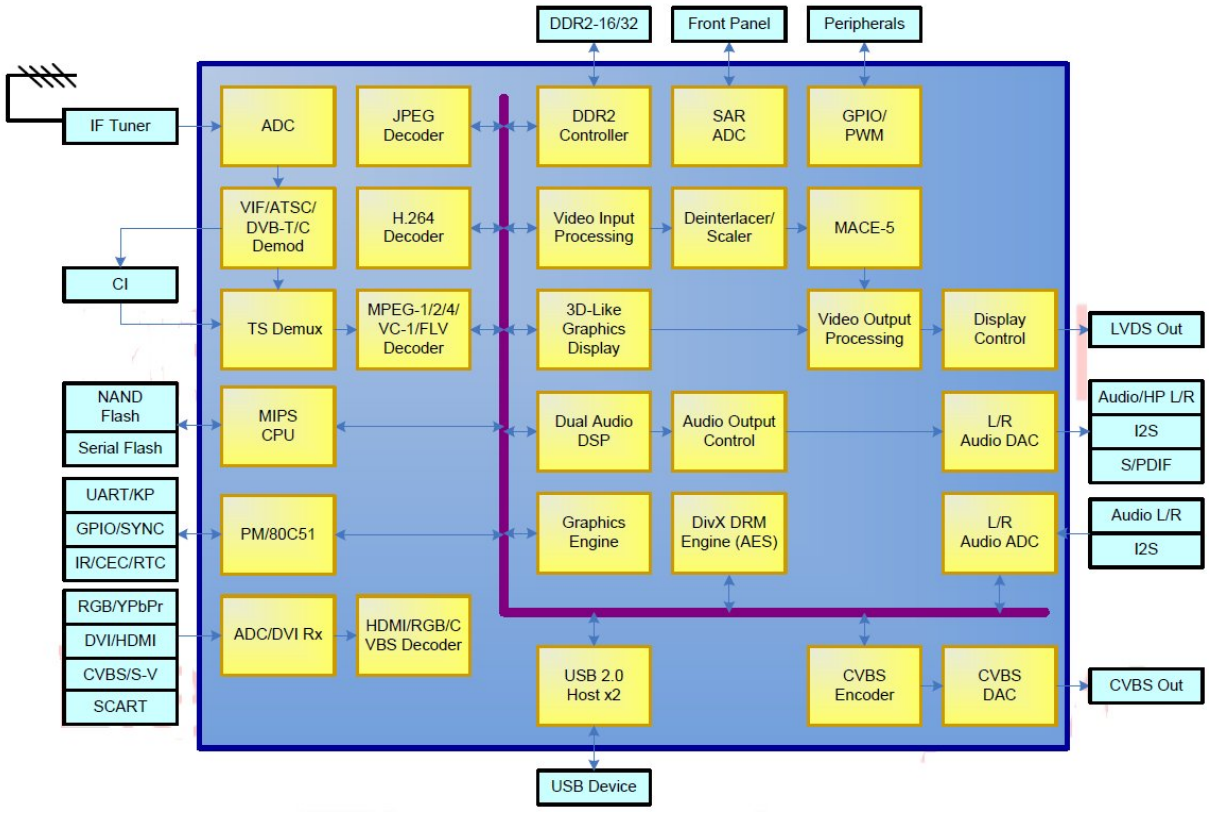
**Connectivity**

- Two USB 2.0 host ports
- USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting

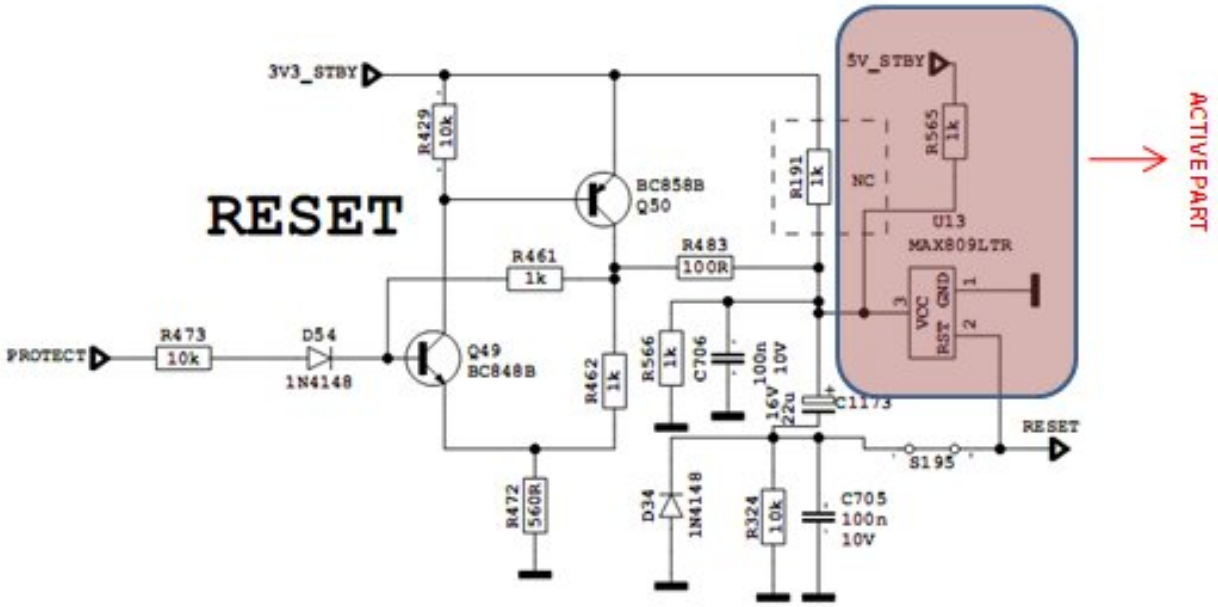
**Miscellaneous**

- DRAM interface supporting two 16-bit DDR2 @ 1066MHz
- Supports PVR
- Supports Common Interface for conditional access support
- Bootable SPI interface with serial flash support
- Parallel interface for external OneNAND and NAND flash support
- Power control module with ultra low power
- MCU available in standby mode
- 523-ball LFBGA package
- Operating Voltages: 1.26V (core), 1.8V (DDR2), 2.5V and 3.3V (I/O and analog)

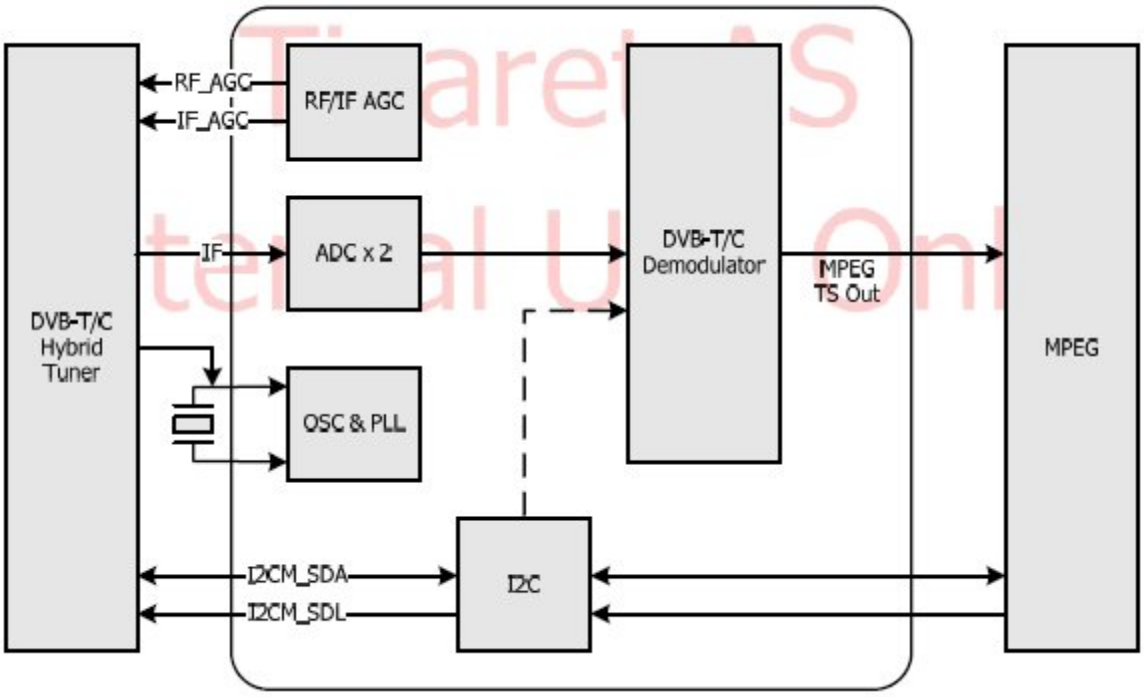
## 4.3. MSTAR Block Diagram



### 4.4. Reset Circuit



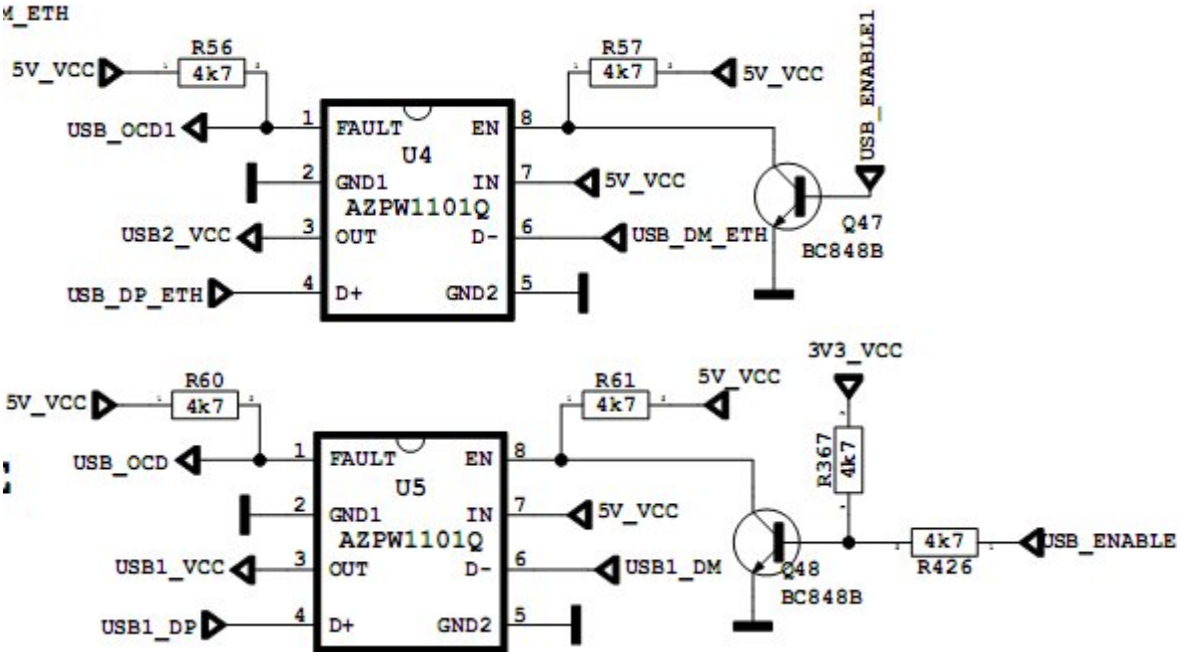

## 5. CI INTERFACE



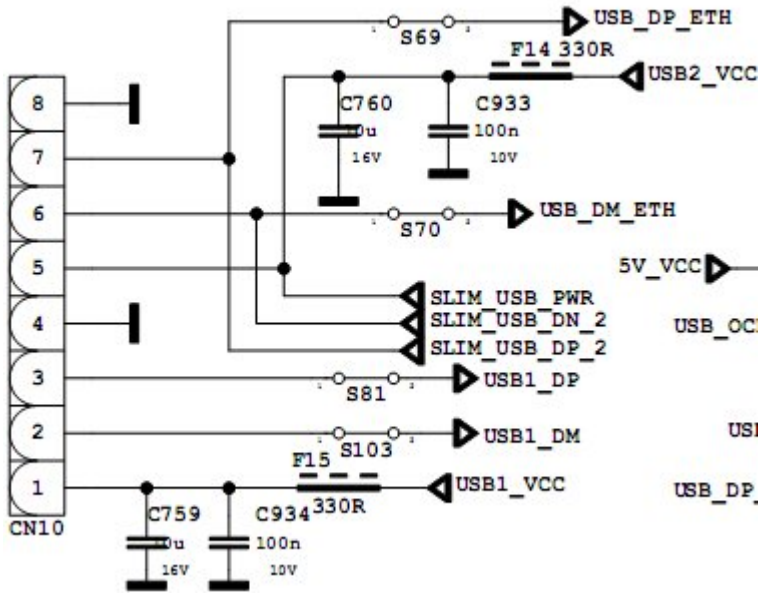
# 6. USB INTERFACE

Main Concept IC has integrated 2 USB 2.0 interface. Two of them is used for USB connectivity for last user. Last user can play video, picture and audio files. Also digital channels can be record to external storage device by this interface. All SW files can be updated with interface.

MB65 USB circuit has power switches (U4- U5) and these are shown below ;




USB connector ;



# 7. DDR2 SDRAM 8M × 4 BANKS × 16 BIT (W9751G6JB) (U11)

## 7.1. General Description

The W9751G6JB is a 512M bits DDR2 SDRAM, organized as 8,388,608 words × 4 banks × 16 bits. This device achieves high speed transfer rates up to 1066Mb/sec/pin (DDR2-1066) for general applications. W9751G6JB is sorted into the following speed grades: -18, -25 and -3. The -18 is compliant to the DDR2-1066/CL7 specification. The -25 is compliant to the DDR2-800 (5-5-5) or DDR2-800 (6-6-6) specification. The -3 is compliant to the DDR2-667 (5-5-5) specification. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CLK rising and CLK falling). All I/Os are synchronized with a single ended DQS or differential DQS- DQS pair in a source synchronous fashion.

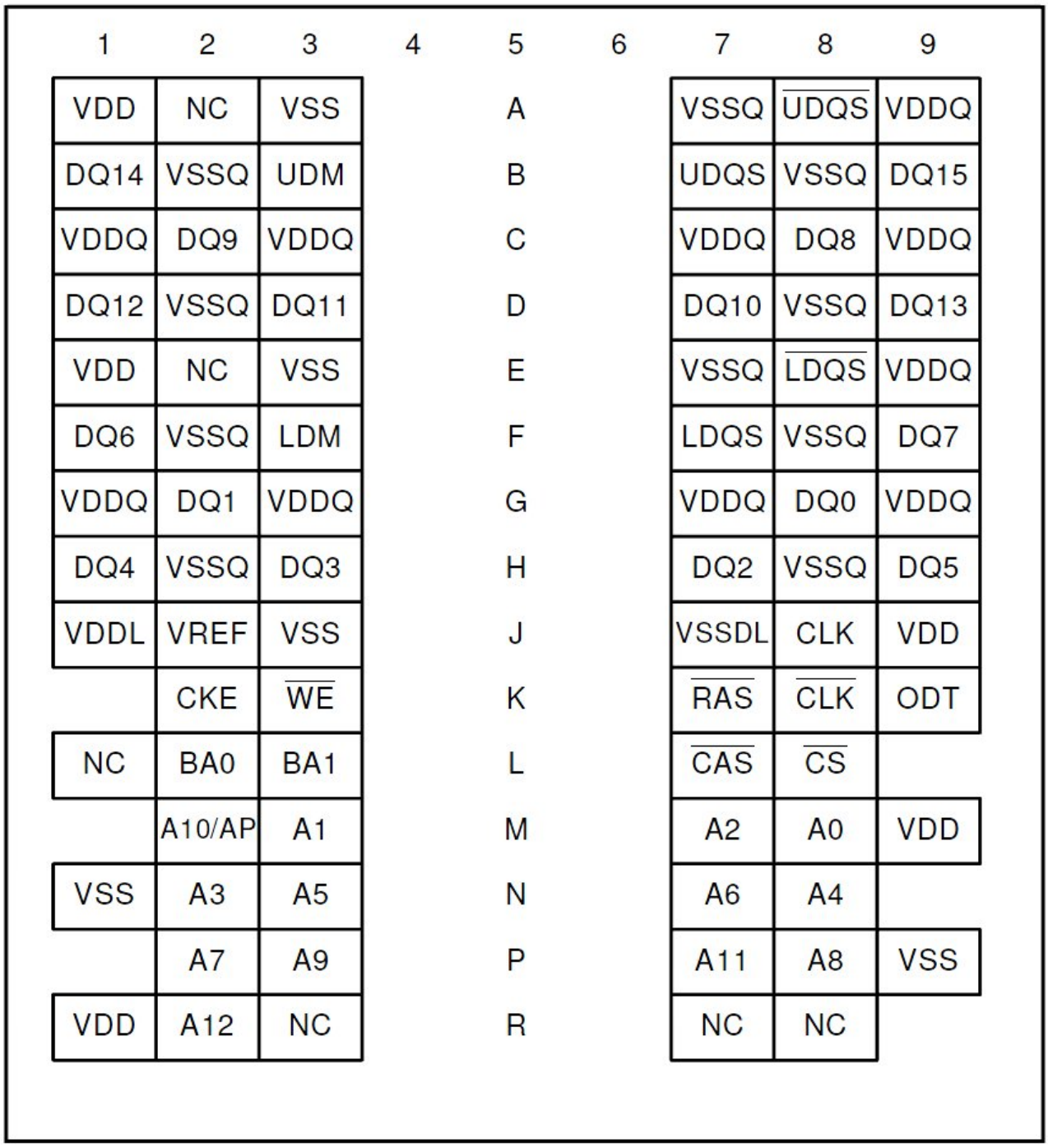
## 7.2. Features

- Power Supply: VDD, VDDQ = 1.8 V± 0.1 V
- Double Data Rate architecture: two data transfers per clock cycle
- CAS Latency: 3, 4, 5, 6 and 7
- Burst Length: 4 and 8
- Bi-directional, differential data strobes (DQS andDQS ) are transmitted / received with data
- Edge-aligned with Read data and center-aligned with Write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CLK and CLK )
- Data masks (DM) for write data
- Commands entered on each positive CLK edge, data and data mask are referenced to both edges of DQS
- Posted CAS programmable additive latency supported to make command and data bus efficiency
- Read Latency = Additive Latency plus CAS Latency (RL = AL + CL)
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality
- Auto-precharge operation for read and write bursts
- Auto Refresh and Self Refresh modes
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)
- Interface: SSTL_18

## 7.3. Electrical Characteristics

| SYM. | PARAMETER | MIN. | TYP. | MAX. | UNIT | NOTES |
|---|---|---|---|---|---|---|
| VDD | Supply Voltage | 1.7 | 1.8 | 1.9 | V | 1 |
| VDDL | Supply Voltage for DLL | 1.7 | 1.8 | 1.9 | V | 5 |
| VDDQ | Supply Voltage for Output | 1.7 | 1.8 | 1.9 | V | 1, 5 |
| VREF | Input Reference Voltage | 0.49 x VDDQ | 0.5 x VDDQ | 0.51 x VDDQ | V | 2, 3 |
| VTT | Termination Voltage (System) | VREF - 0.04 | VREF | VREF + 0.04 | V | 4 |

### 7.4. Pinning



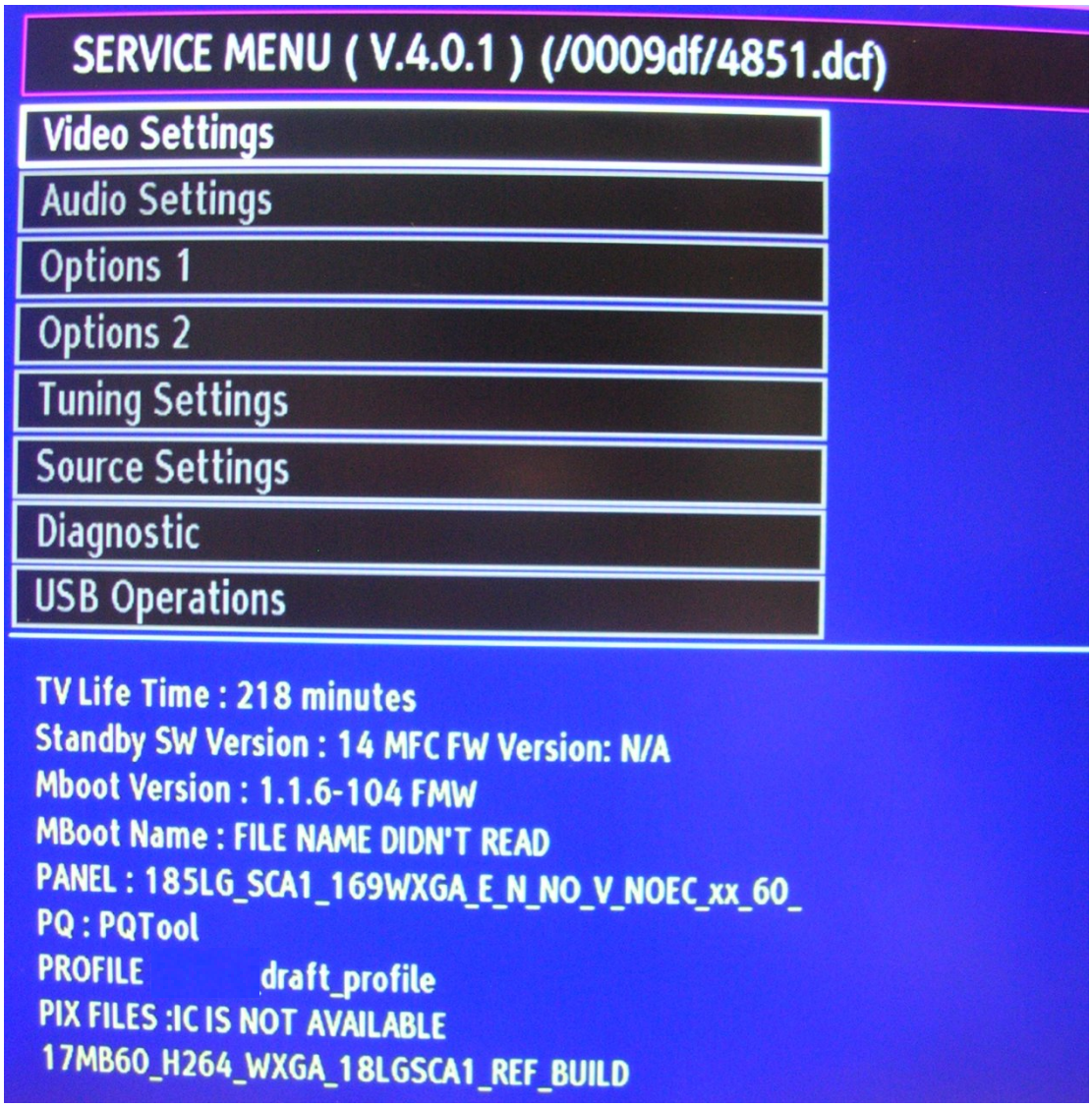
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|
| VDD | NC | VSS | | A | | VSSQ | $\overline{\text{UDQS}}$ | VDDQ |
| DQ14 | VSSQ | UDM | | B | | UDQS | VSSQ | DQ15 |
| VDDQ | DQ9 | VDDQ | | C | | VDDQ | DQ8 | VDDQ |
| DQ12 | VSSQ | DQ11 | | D | | DQ10 | VSSQ | DQ13 |
| VDD | NC | VSS | | E | | VSSQ | $\overline{\text{LDQS}}$ | VDDQ |
| DQ6 | VSSQ | LDM | | F | | LDQS | VSSQ | DQ7 |
| VDDQ | DQ1 | VDDQ | | G | | VDDQ | DQ0 | VDDQ |
| DQ4 | VSSQ | DQ3 | | H | | DQ2 | VSSQ | DQ5 |
| VDDL | VREF | VSS | | J | | VSSDL | CLK | VDD |
| | CKE | $\overline{\text{WE}}$ | | K | | $\overline{\text{RAS}}$ | $\overline{\text{CLK}}$ | ODT |
| NC | BA0 | BA1 | | L | | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$ | |
| | A10/AP | A1 | | M | | A2 | A0 | VDD |
| VSS | A3 | A5 | | N | | A6 | A4 | |
| | A7 | A9 | | P | | A11 | A8 | VSS |
| VDD | A12 | NC | | R | | NC | NC | |

| BALL NUMBER | SYMBOL | FUNCTION | DESCRIPTION |
|---|---|---|---|
| M8,M3,M7,N2,N8,N3,N7,P2,P8,P3,M2,P7,R2 | A0–A12 | Address | Provide the row address for active commands, and the column address and Auto-precharge bit for Read/Write commands to select one location out of the memory array in the respective bank.<br>Row address: A0–A12.<br>Column address: A0–A9. (A10 is used for Auto-precharge) |
| L2,L3 | BA0–BA1 | Bank Select | BA0–BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied. |
| G8,G2,H7,H3,H1,H9,F1,F9,C8,C2,D7,D3,D1,D9,B1,B9 | DQ0–DQ15 | Data Input / Output | Bi-directional data bus. |
| K9 | ODT | On Die Termination Control | ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. |
| F7,E8 | LDQS, $\overline{\text{LDQS}}$ | LOW Data Strobe | Data Strobe for Lower Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS corresponds to the data on DQ0–DQ7. $\overline{\text{LDQS}}$ is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command]. |
| B7,A8 | UDQS, $\overline{\text{UDQS}}$ | UP Data Strobe | Data Strobe for Upper Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS corresponds to the data on DQ8–DQ15. $\overline{\text{UDQS}}$ is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command]. |
| L8 | $\overline{\text{CS}}$ | Chip Select | All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple ranks. $\overline{\text{CS}}$ is considered part of the command code. |
| K7,L7,K3 | $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ | Command Inputs | $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$ ) define the command being entered. |
| B3,F3 | UDM<br>LDM | Input Data Mask | DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. |
| J8,K8 | CLK, $\overline{\text{CLK}}$ | Differential Clock Inputs | CLK and $\overline{\text{CLK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of $\overline{\text{CLK}}$ . Output (read) data is referenced to the crossings of CLK and $\overline{\text{CLK}}$ (both directions of crossing). |
| K2 | CKE | Clock Enable | CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. |
| J2 | $V_{REF}$ | Reference Voltage | $V_{REF}$ is reference voltage for inputs. |
| A1,E1,J9,M9,R1 | $V_{DD}$ | Power Supply | Power Supply: 1.8V ± 0.1V. |
| A3,E3,J3,N1,P9 | $V_{SS}$ | Ground | Ground. |
| A9,C1,C3,C7,C9,E9,G1,G3,G7,G9 | $V_{DDQ}$ | DQ Power Supply | DQ Power Supply: 1.8V ± 0.1V. |
| A7,B2,B8,D2,D8,E7,F2,F8,H2,H8 | $V_{SSQ}$ | DQ Ground | DQ Ground. Isolated on the device for improved noise immunity. |
| A2,E2,L1,R3,R7,R8 | NC | No Connection | No connection. |
| J7 | $V_{SSDL}$ | DLL Ground | DLL Ground. |
| J1 | $V_{DDL}$ | DLL Power Supply | DLL Power Supply: 1.8V ± 0.1V. |

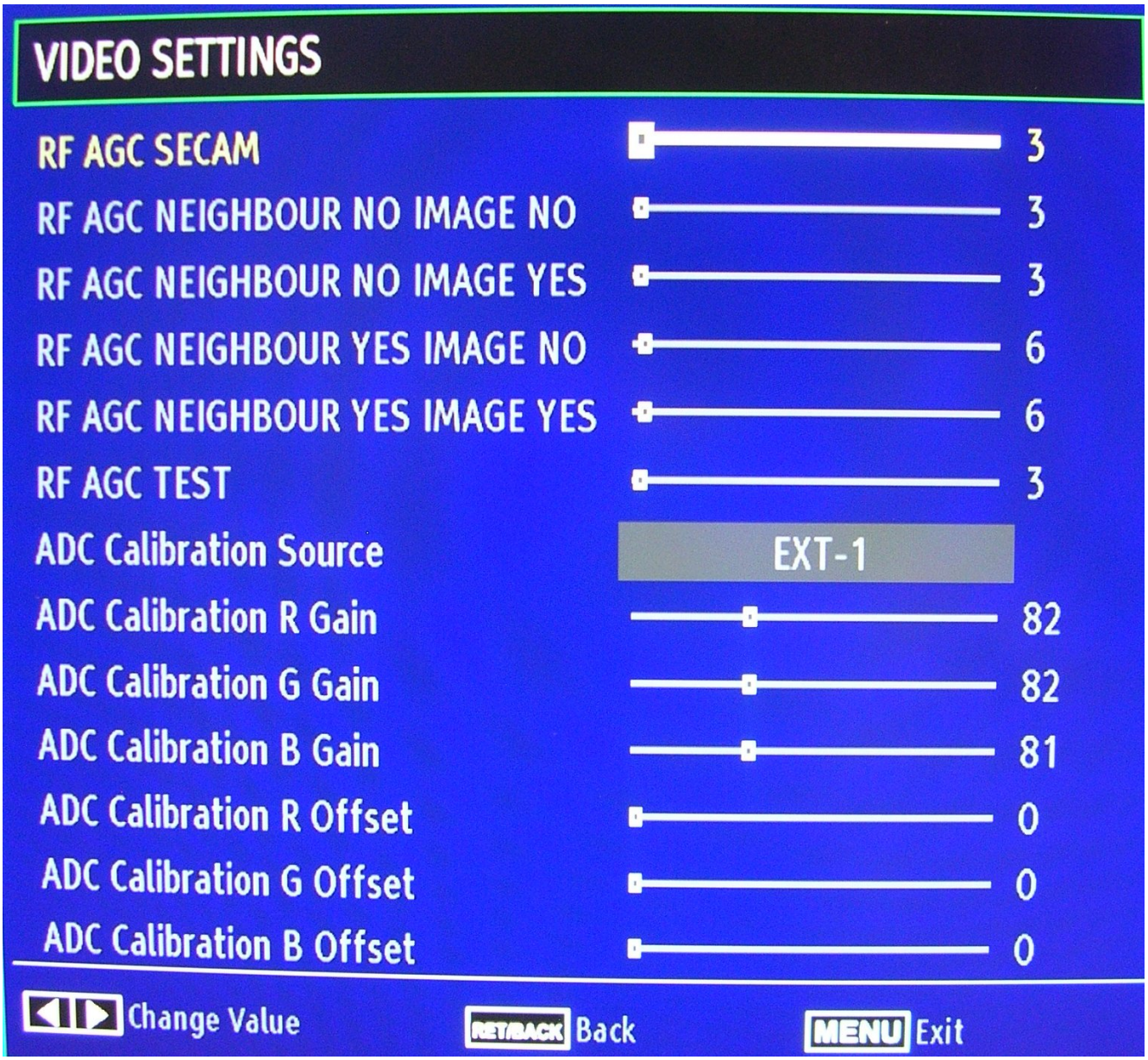
# 8. SERVICE MENU SETTINGS

In order to reach service menu,  First Press **“MENU”** Then press the remote control code two times, which is **“4725”**.

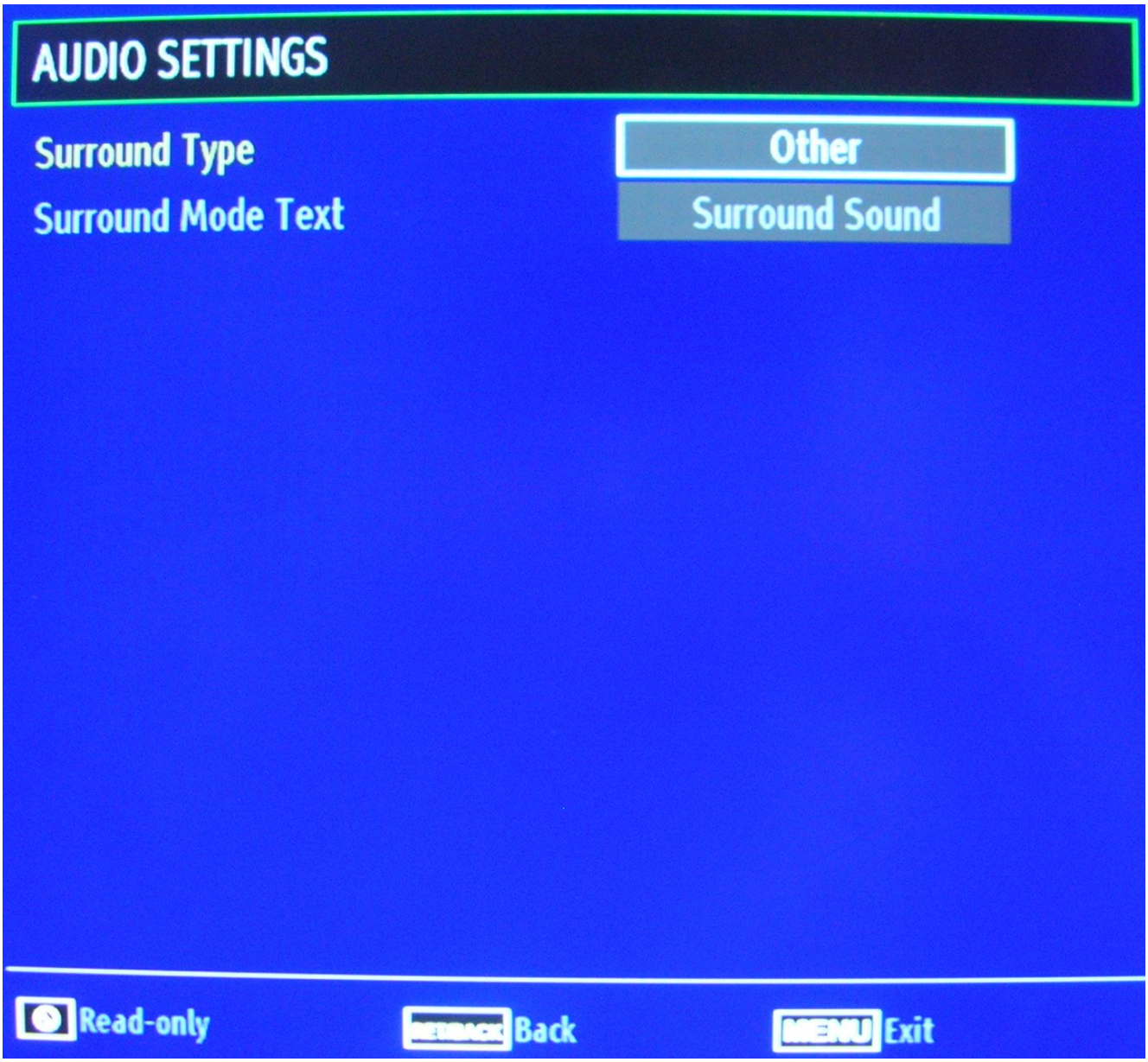
In first screen following items can be seen:



## 8.1. Video Settings

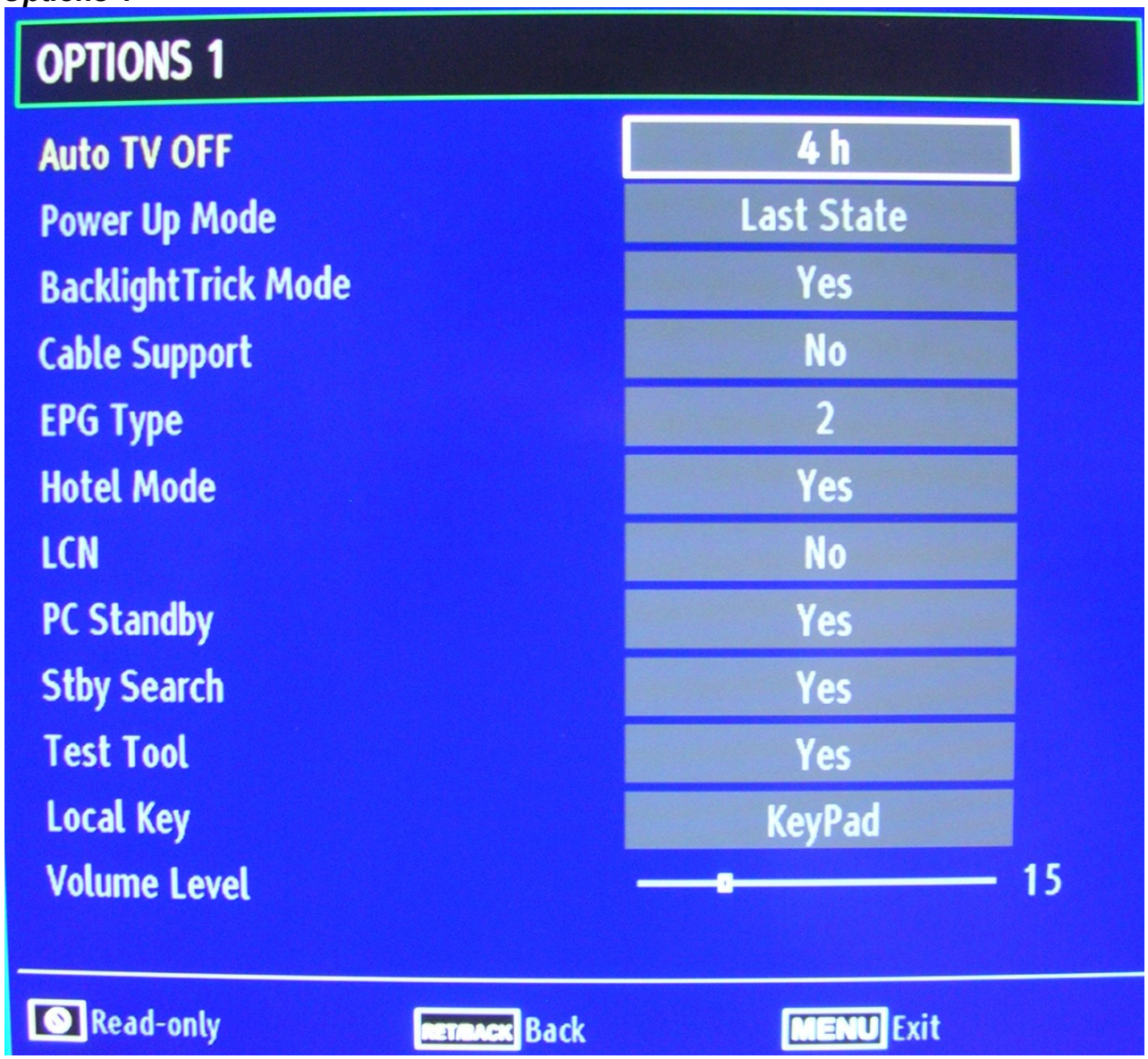


## 8.2. Audio Settings

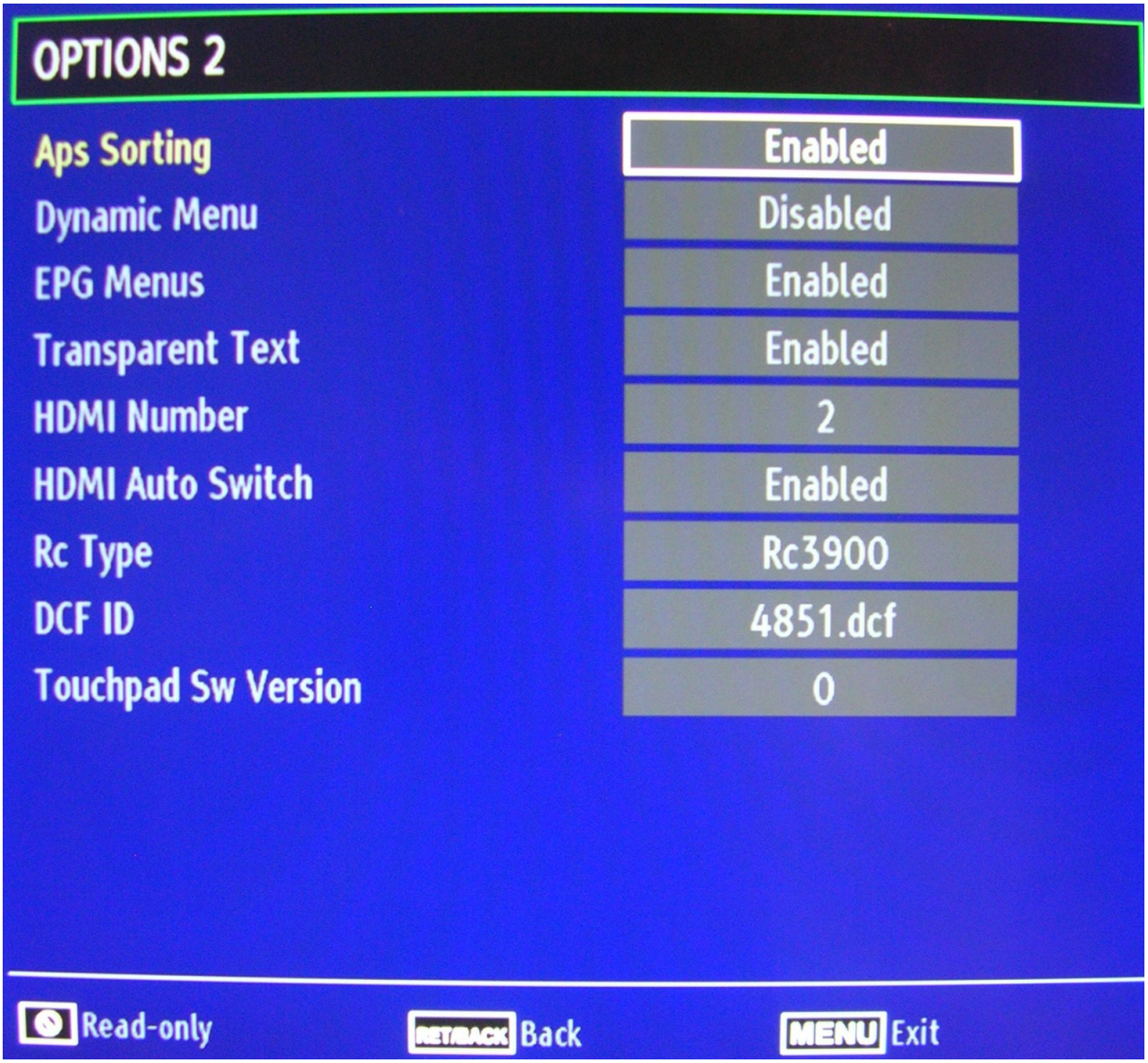


## 8.3. Options

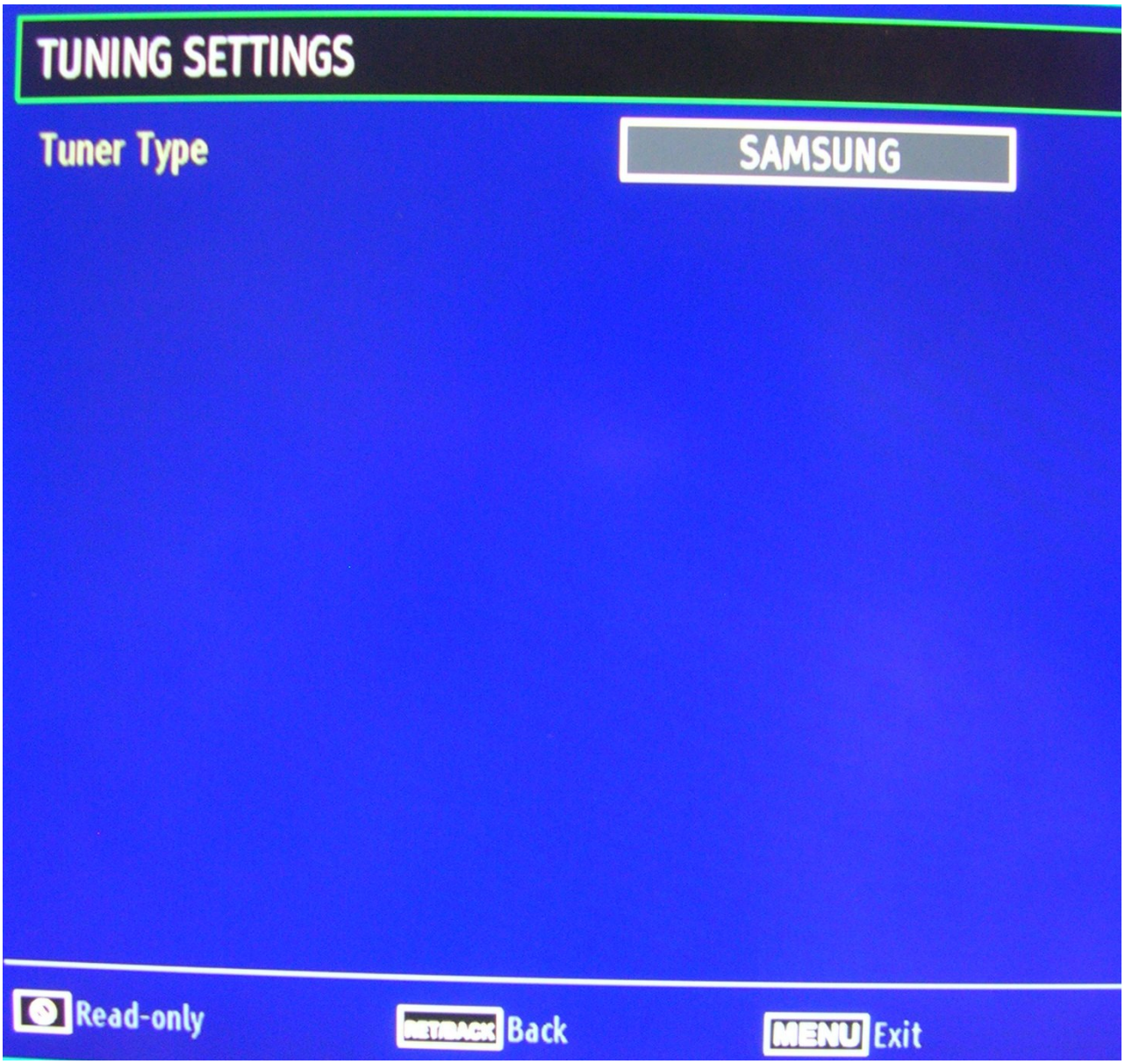
*Options-1*



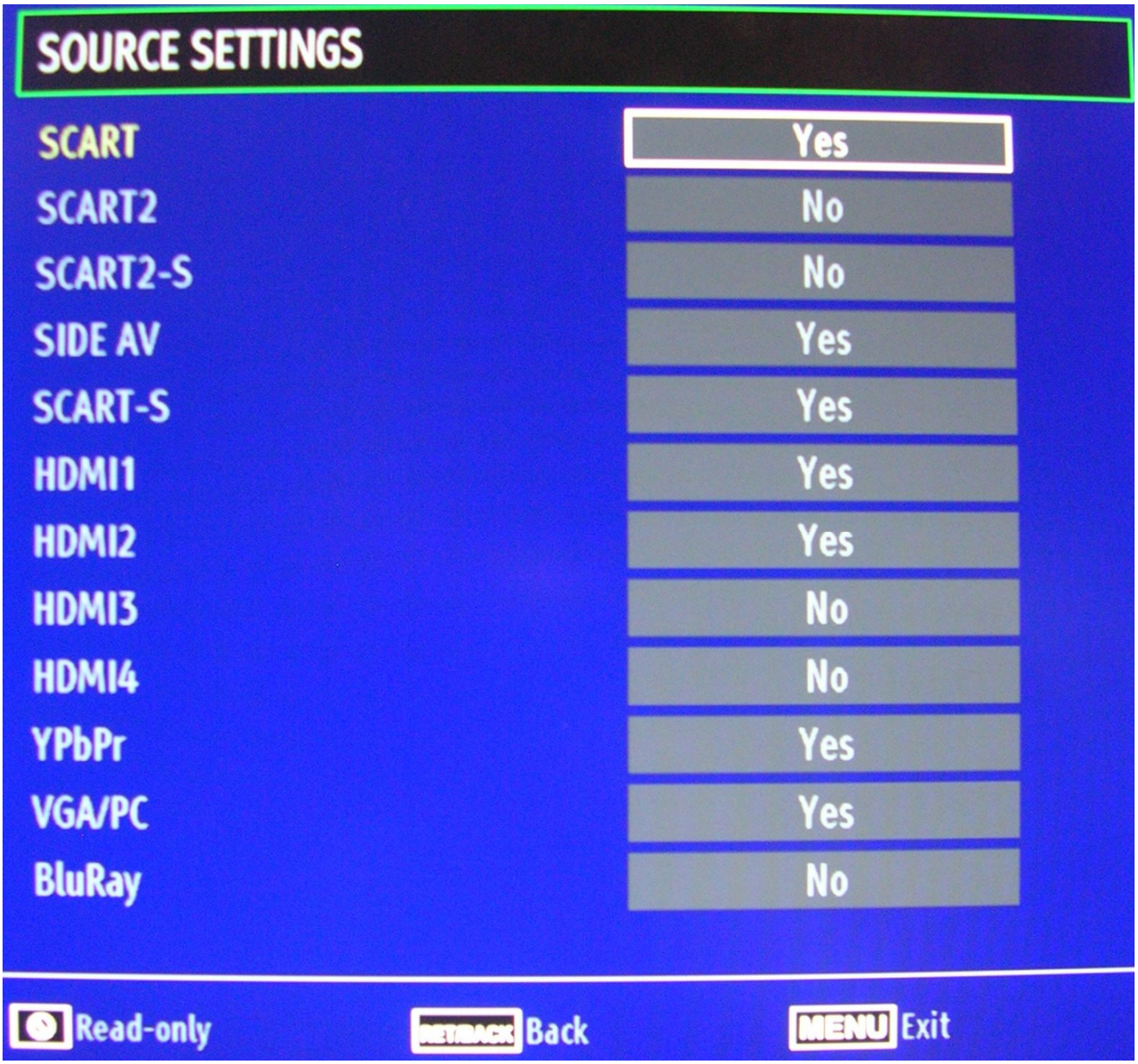
***Options-2***


OPTIONS 2
Aps Sorting
Enabled
Dynamic Menu
Disabled
EPG Menus
Enabled
Transparent Text
Enabled
HDMI Number
2
HDMI Auto Switch
Enabled
Rc Type
Rc3900
DCF ID
4851.dcf
Touchpad Sw Version
0
Read-only
RETURN/BACK Back
MENU Exit

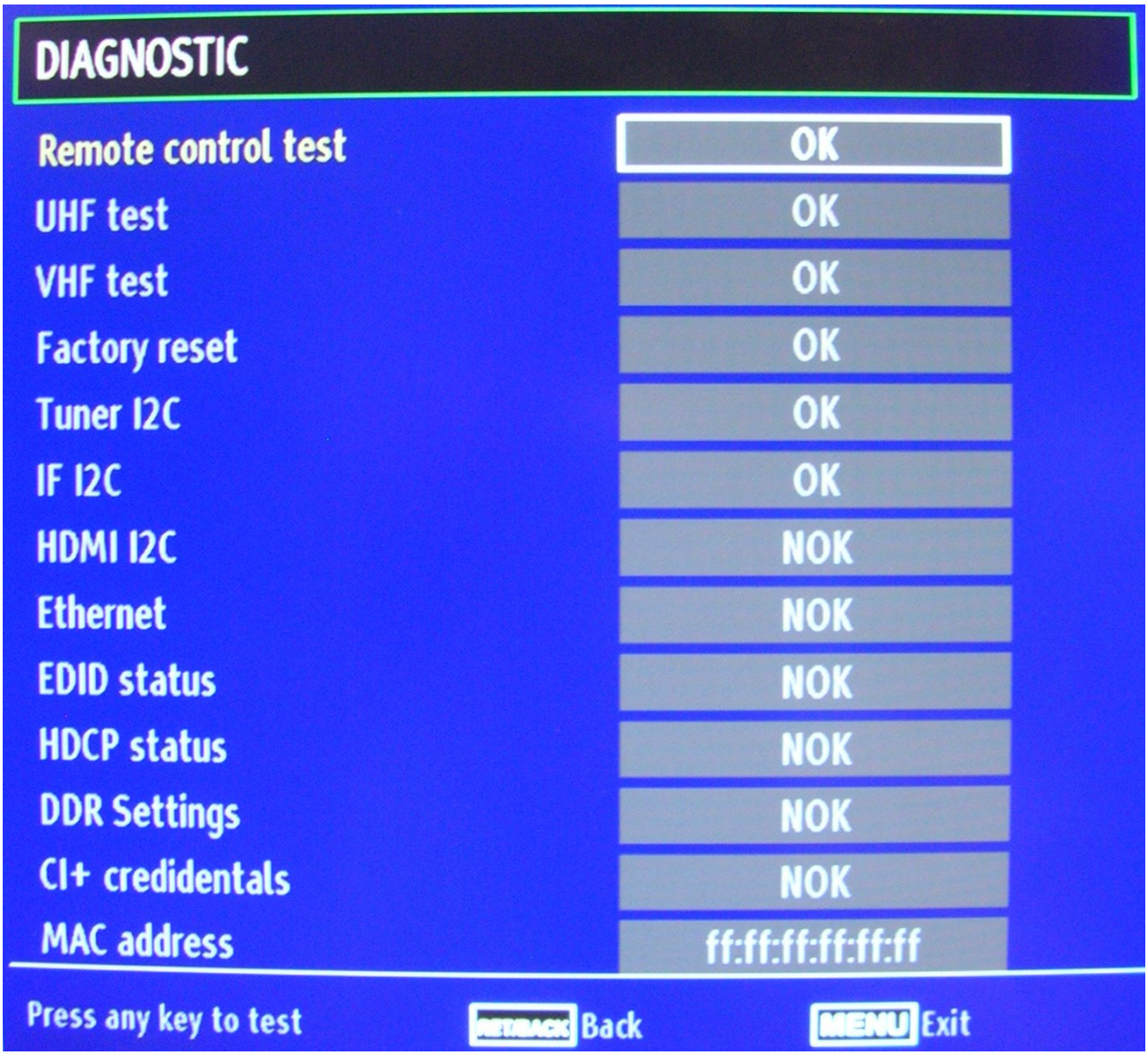
## 8.4. Tuning Settings



## 8.5. Source Settings



## 8.6. Diagnostic




## 8.7. USB Operations

USB operations option cannot be used directly. It can be used for updating panel tool, hw configuration etc.

# 9. SOFTWARE UPDATE

In MB65 project there is only one software. From following steps software update procedure can be seen:

1. MB65_en.bin, mboot.bin and usb_auto_update_mb65.txt documents should copy directly inside of a flash memory(not in a folder).
2. Insert flash memory to the tv when tv is powered off.
3. Power on the and wait when the tv is opened.
4. Press OK button for a while
5. If First Time Installation screen comes, it means software update procedure is successful.

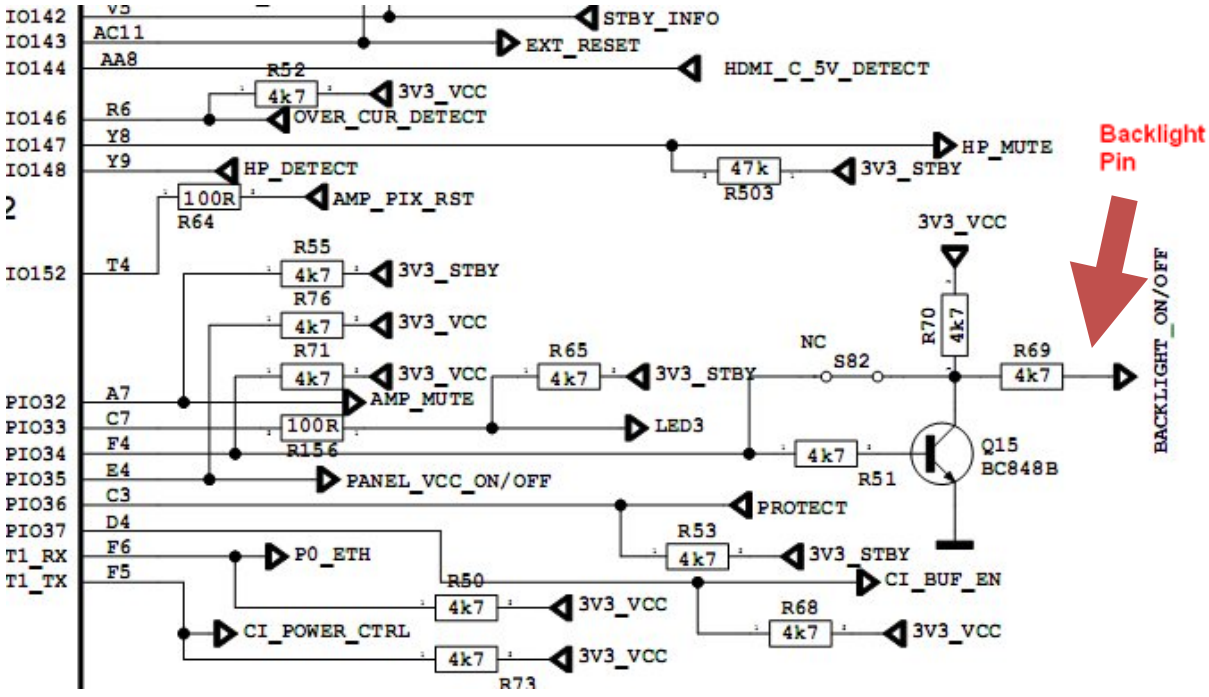
# 10. TROUBLESHOOTING

## 10.1. No Backlight Problem

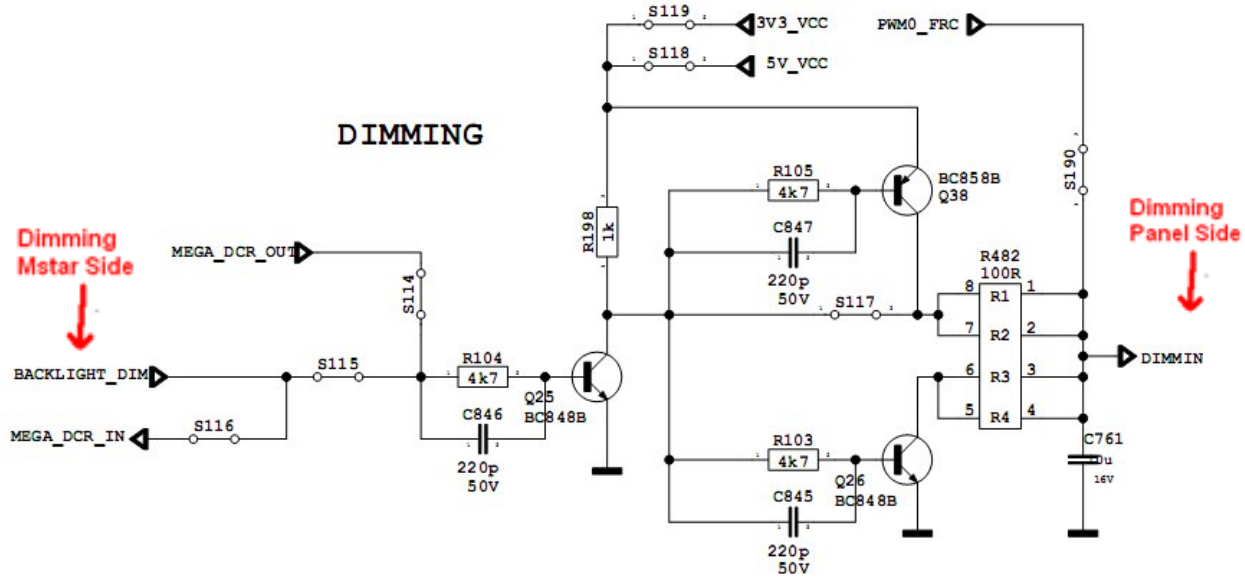
Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible couses: Backlight pin, dimming pin, backlight supply, stby on/off pin

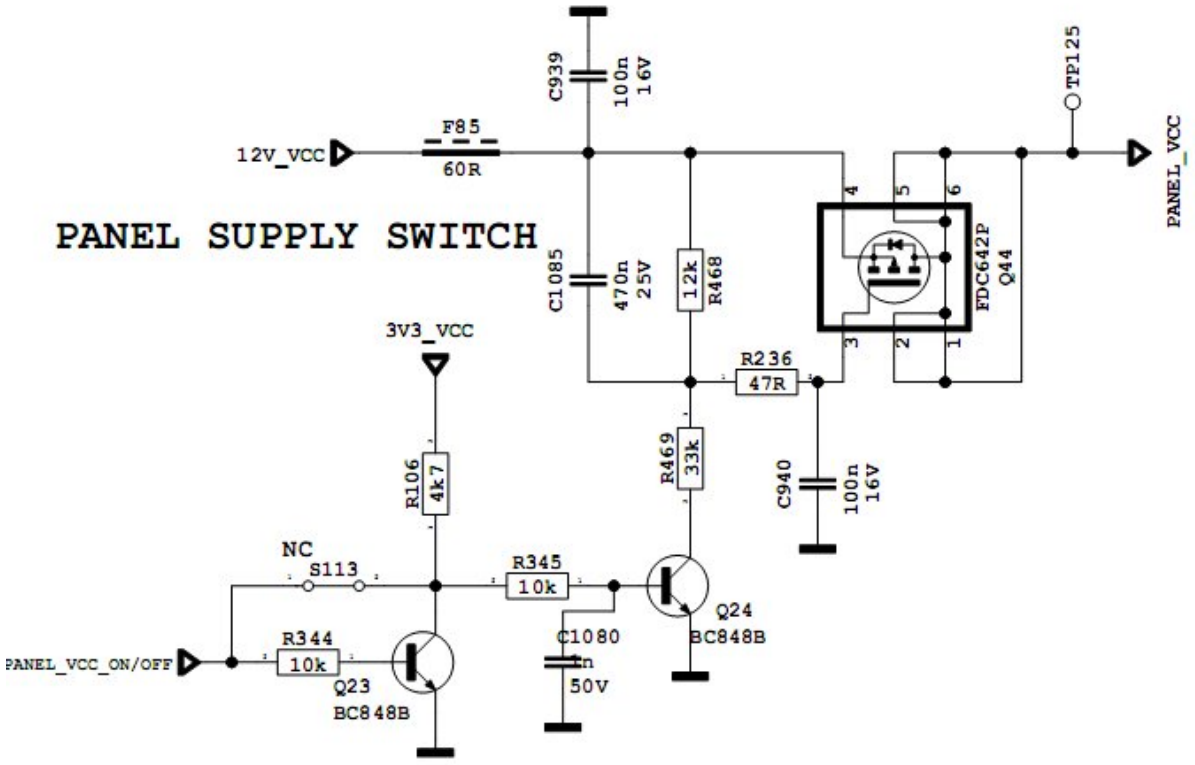
Backlight pin should be high in open position. If it is low, please check Q15 and panel cables.



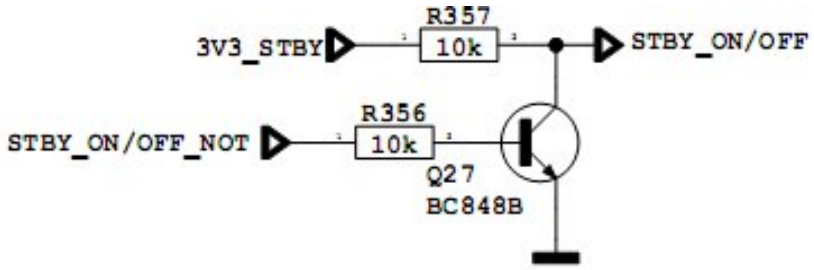
Dimming pin should be high or square wave in open position. If it is low, please check S115 for Mstar side and panel or power cables, connectors.




Backlight power supply should be in panel specs. Please check Q44, shown below;



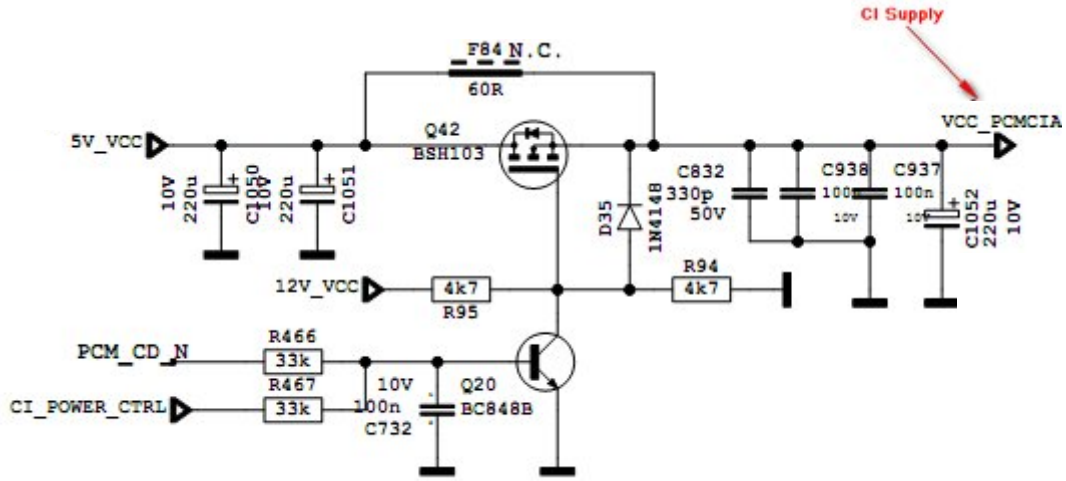
STBY_ON/OFF should be low for tv on condition, please check Q27's collector.




## 10.2. CI Module Problem

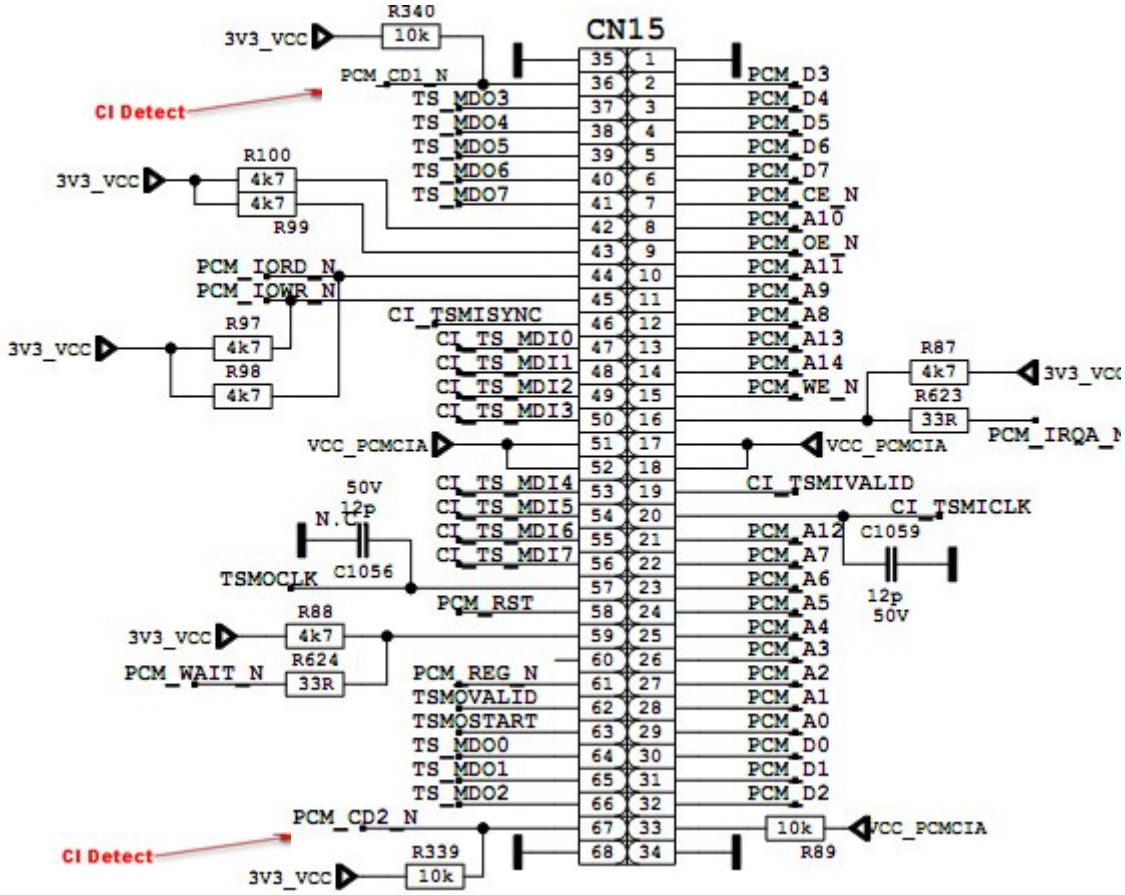
Problem: CI is not working when CI module inserted.

Possible causes: Supply, supply control pin, detect pins, mechanical positions of pins
CI supply should be 5V when CI module inserted. If it is not 5V please check CI_POWER_CTRL, this pin should be low.




Please check mechanical positions of CI module.

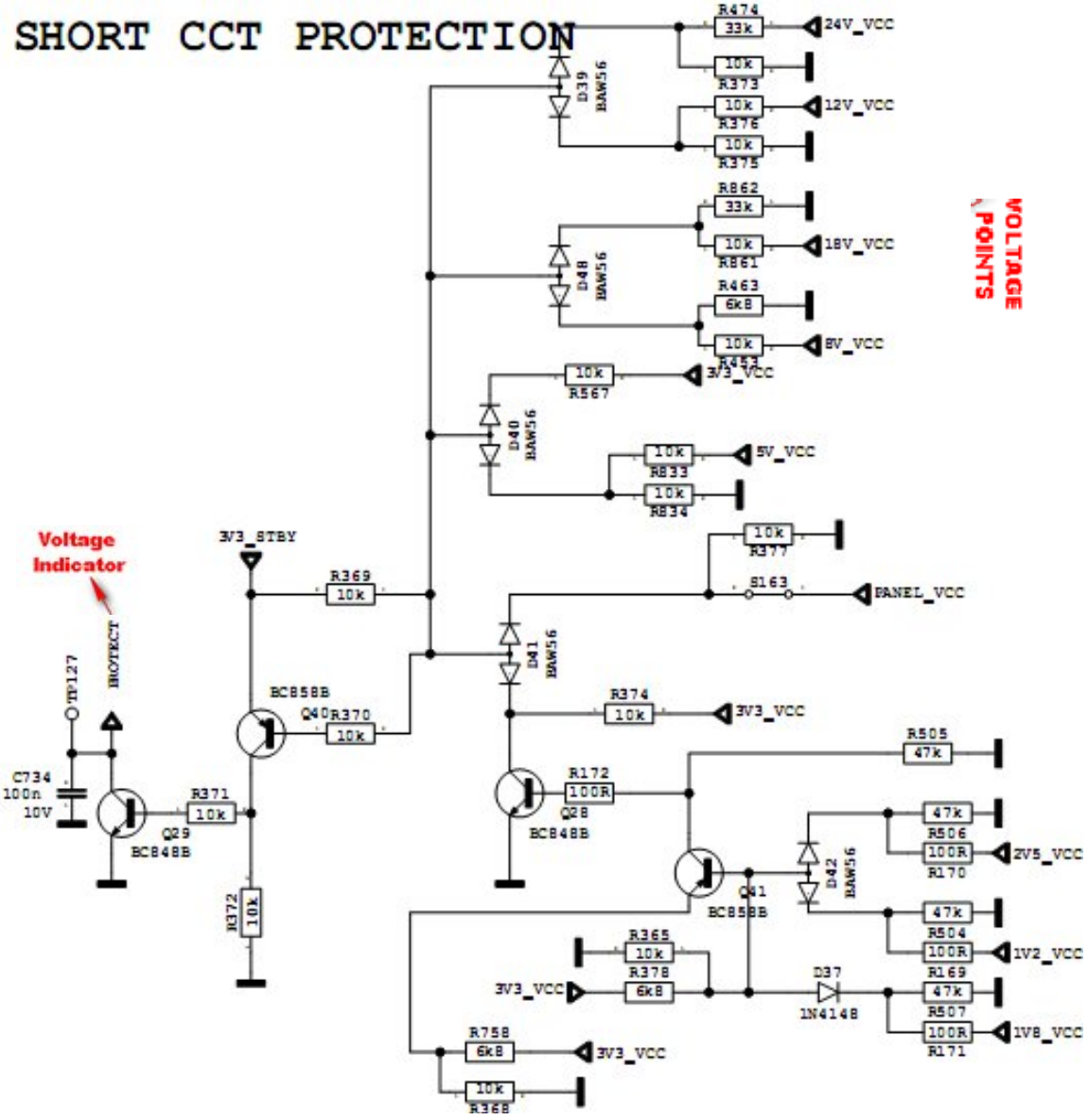
Detect ports should be low. If it is not low please check CI connector pins


CN15
R340
10k
3V3_VCC
PCM_CD1_N
CI Detect
R100
4k7
4k7
R99
R97
4k7
R98
4k7
PCM_IORD_N
PCM_IOWR_N
CI_TSMISYNC
CI_TS_MDI0
CI_TS_MDI1
CI_TS_MDI2
CI_TS_MDI3
VCC_PCMCIA
CI_TS_MDI4
CI_TS_MDI5
CI_TS_MDI6
CI_TS_MDI7
50V
12p
N.C
TSMOCLK
C1056
PCM_RST
R88
4k7
R624
33R
PCM_WAIT_N
PCM_REG_N
TSMOVALID
TSMOSTART
TS_MDO0
TS_MDO1
TS_MDO2
PCM_CD2_N
CI Detect
R339
10k
TS_MDO3
TS_MDO4
TS_MDO5
TS_MDO6
TS_MDO7
PCM_D3
PCM_D4
PCM_D5
PCM_D6
PCM_D7
PCM_CE_N
PCM_A10
PCM_OE_N
PCM_A11
PCM_A9
PCM_A8
PCM_A13
PCM_A14
PCM_WE_N
R87
4k7
R623
33R
PCM_IRQA_N
VCC_PCMCIA
CI_TSMIVALID
CI_TSMICLK
PCM_A12
C1059
12p
50V
PCM_A7
PCM_A6
PCM_A5
PCM_A4
PCM_A3
PCM_A2
PCM_A1
PCM_A0
PCM_D0
PCM_D1
PCM_D2
10k
R89
VCC_PCMCIA

## 10.3. Led Blinking Problem

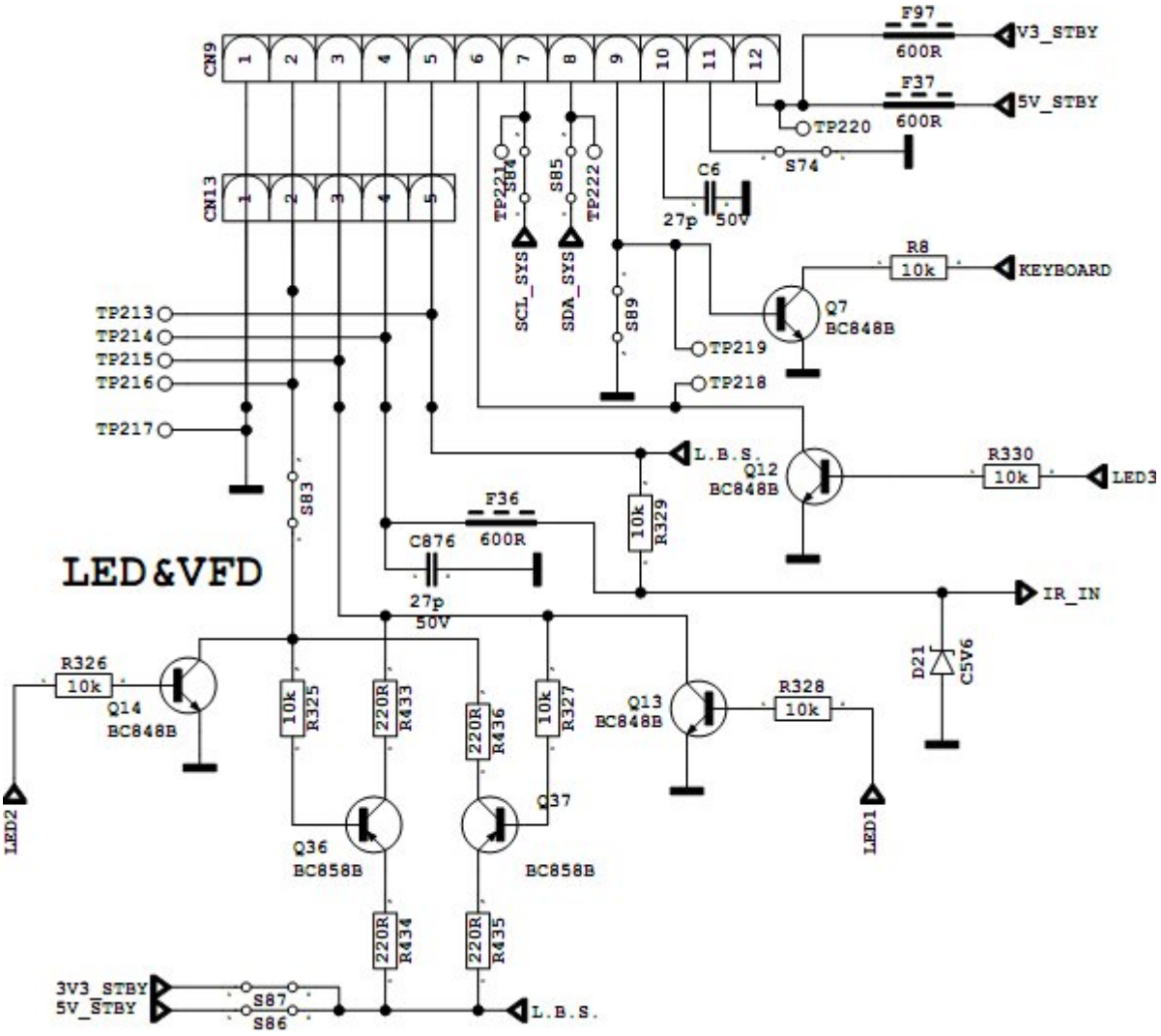
Problem: LED blinking, no other operation

This problem indicates a short on Vcc voltages. Protect pin should be logic high while normal operation. When there is a short circuit protect pin will be logic low. If you detect logic low on protect pin, unplug the TV set and control voltage points with a



## 10.4. IR Problem

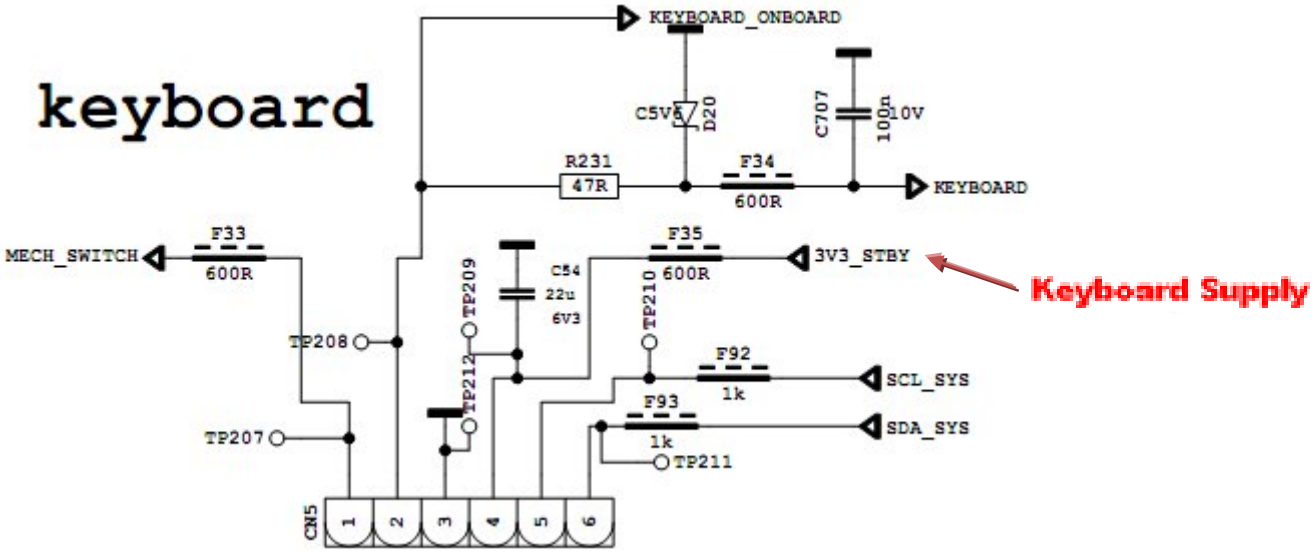
Problem: LED or IR not working
Check LED card supply on MB65 chasis



## 10.5. Keypad Touchpad Problems

Problem: Keypad or Touchpad is not working

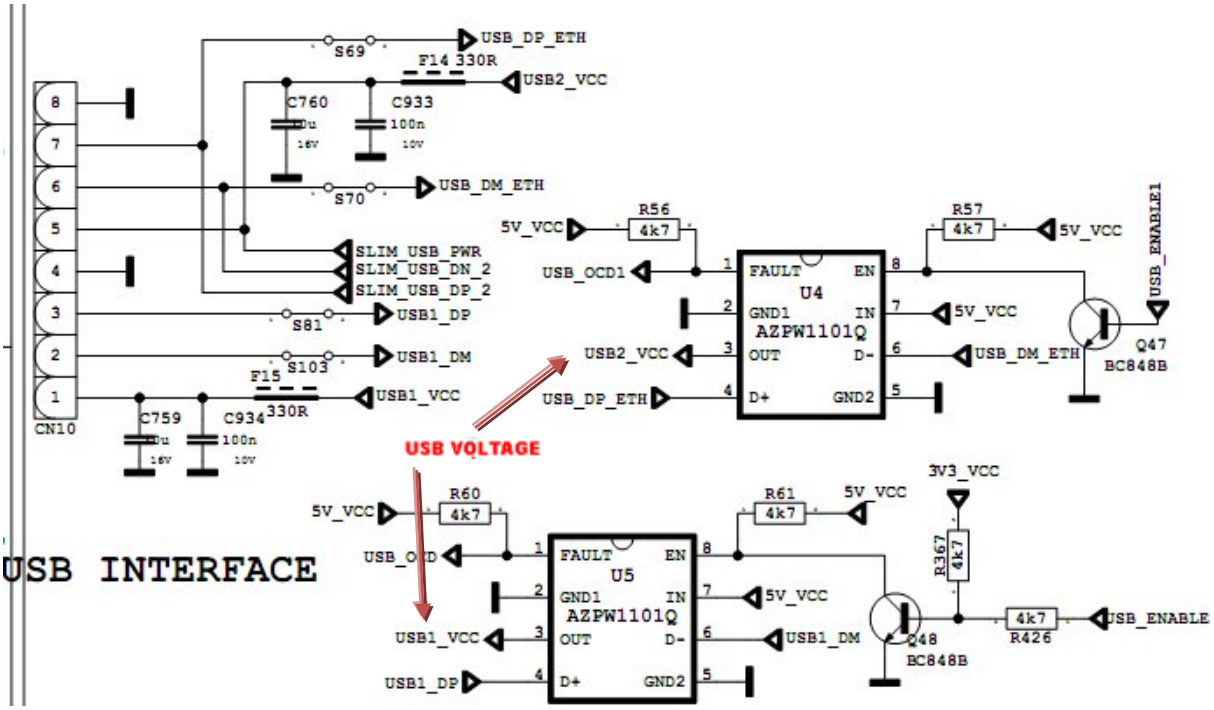
Check keypad supply and KEYBOARD pin on MB65



## 10.6. USB Problems

Problem: USB is not working or no USB Detection.

Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high

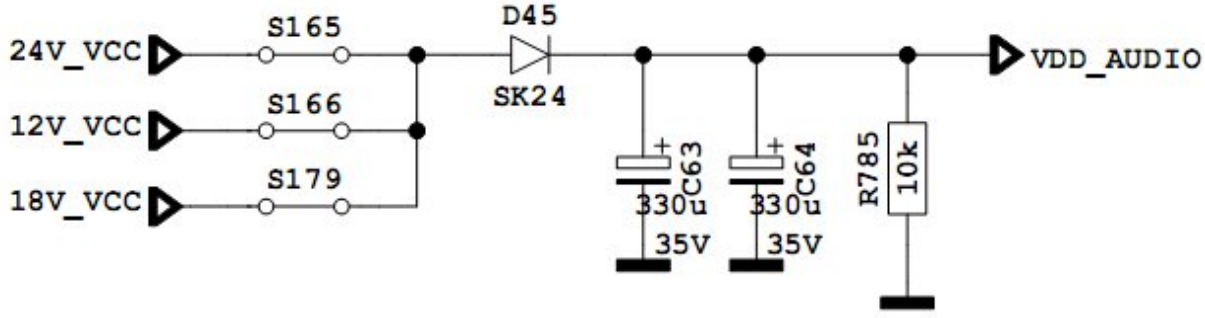



## 10.7. No Sound Problem

Problem: No audio at main TV speaker outputs.

Check supply voltages of VDD_AUDIO.

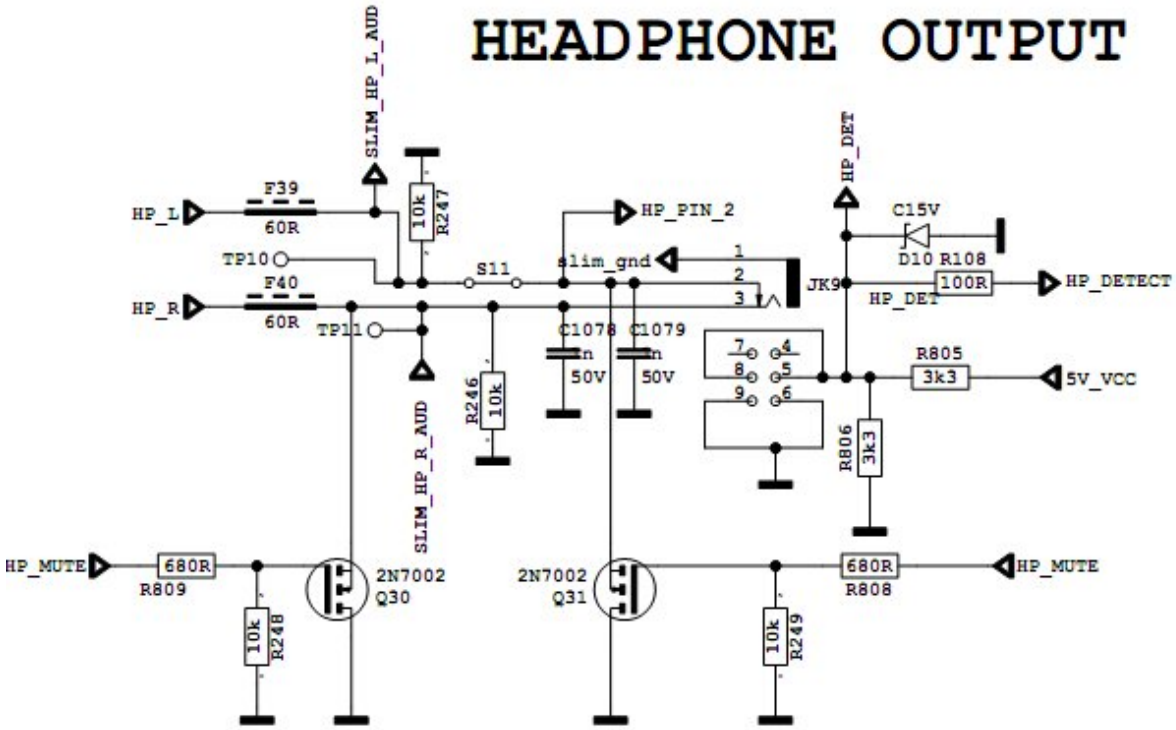
There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 2.5V for MB65.



## 10.8. No Sound Problem at Headphone

Problem: No audio at headphone output.

Check HP detect pin, when headphone is on. It should be 0V




## 10.9. Standby On/Off Problem

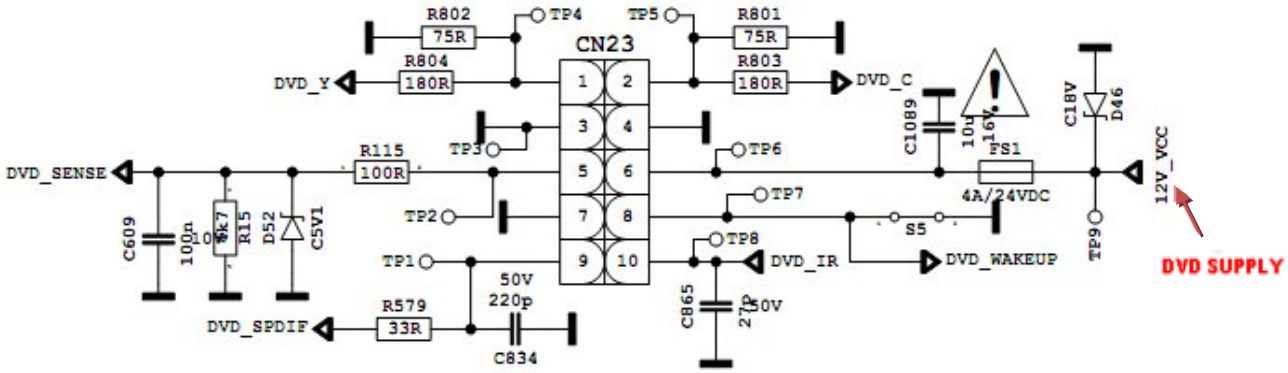
Problem:Device cannot boot, TV hangs in standby mode.

There may be a problem about power supply. Check powers with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via hyper-terminal (or Teraterm). These printouts may give a clue about the problem.

## DVD Problems

Problem: DVD is not working.

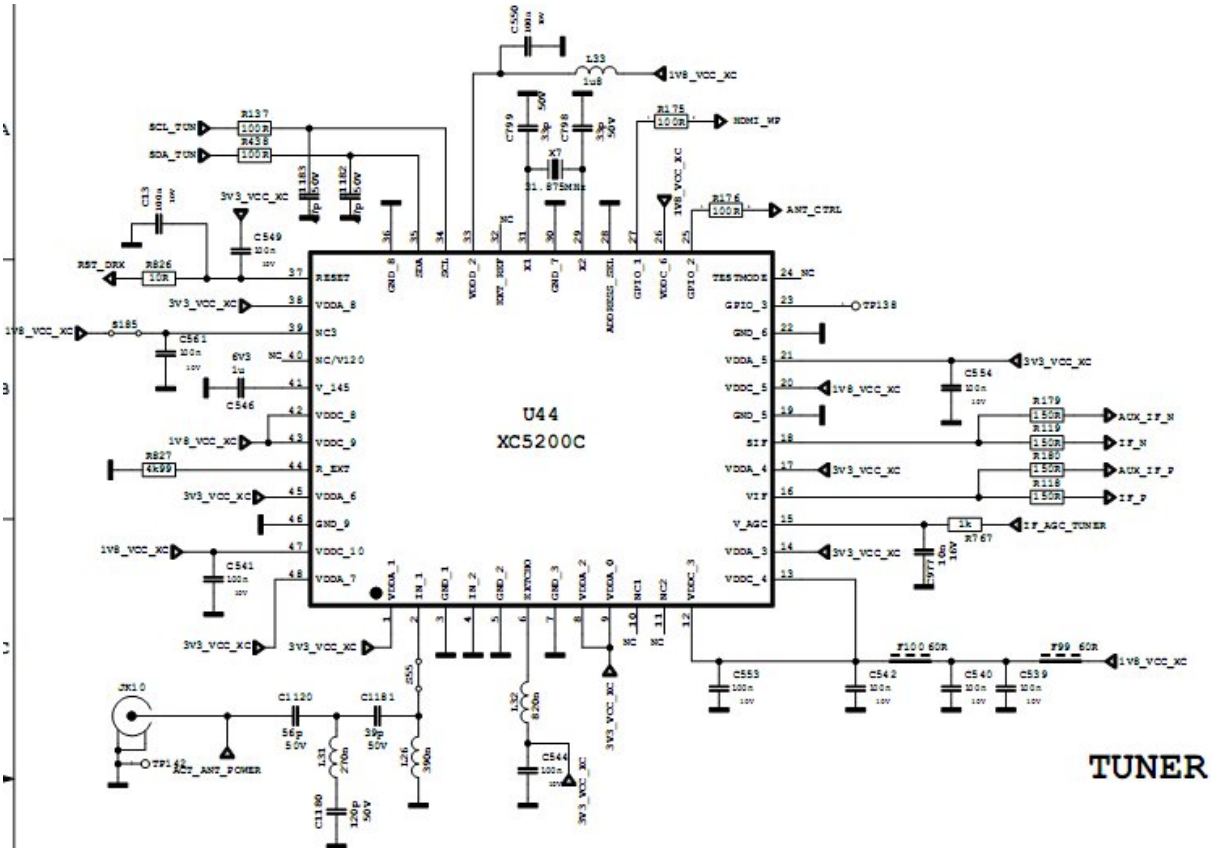
Check that DVD source is selected in Service menu. Check supply voltage of DVD namely 12V_VCC.

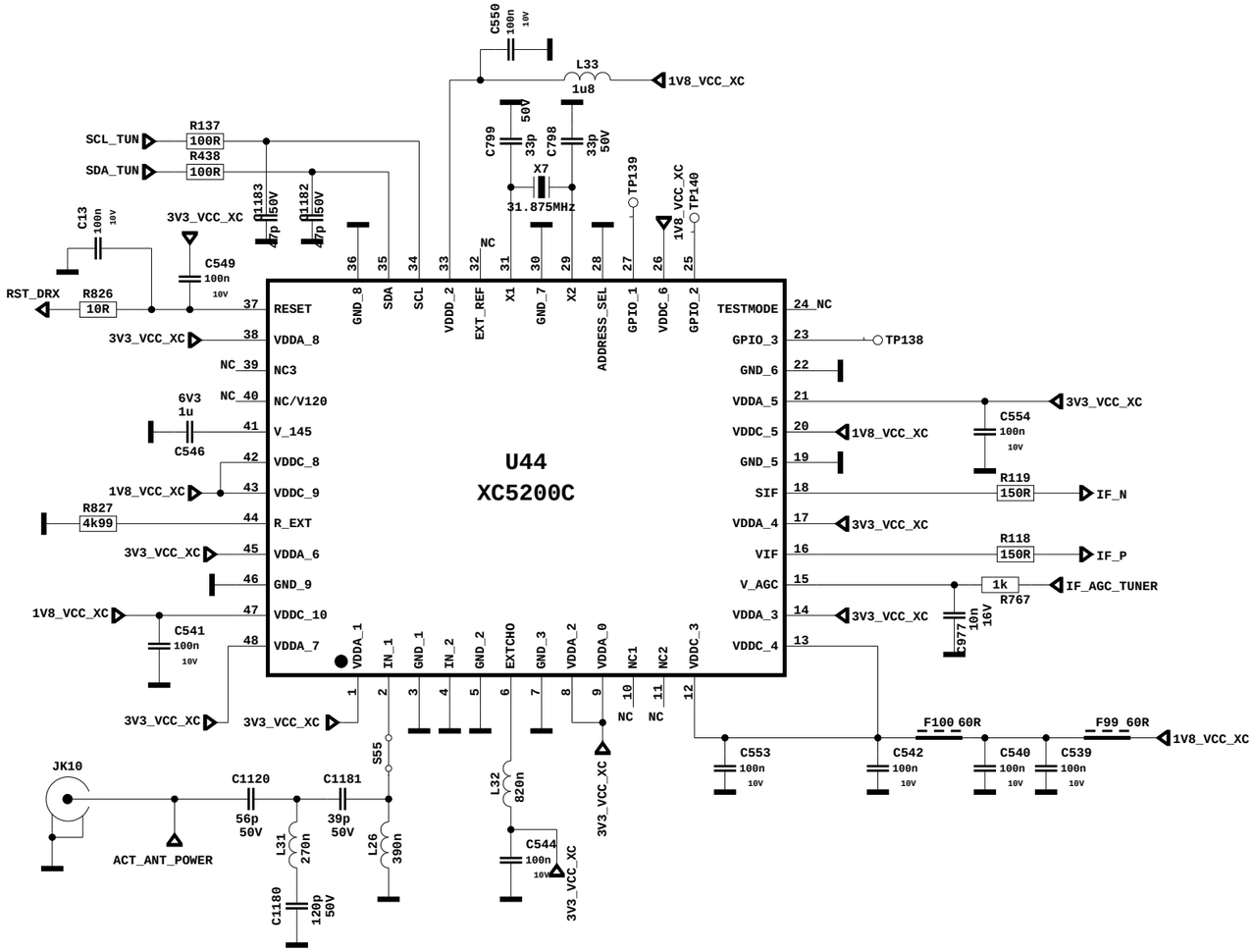


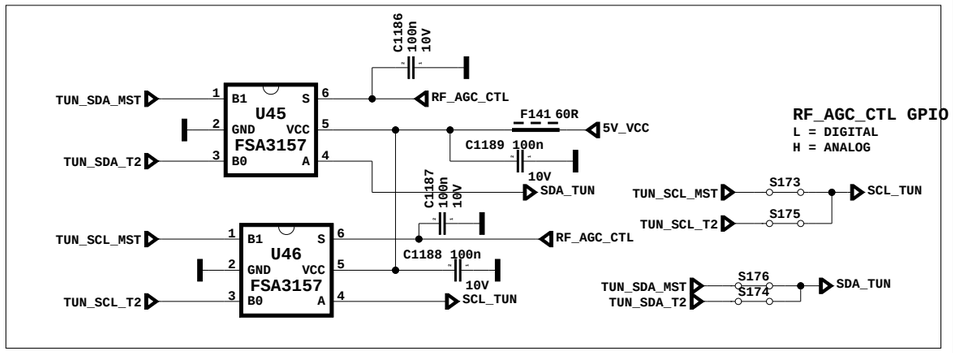
## 10.10. No Signal Problem

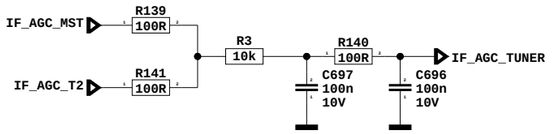
Problem: No signal in TV mode.

Check tuner supply voltage; 3V3_VCC_XC and 1V8_VCC_XC. Check tuner options are correctly set in Service menu.



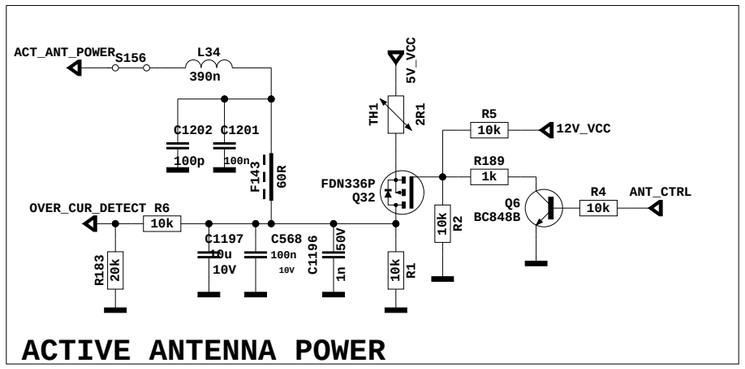


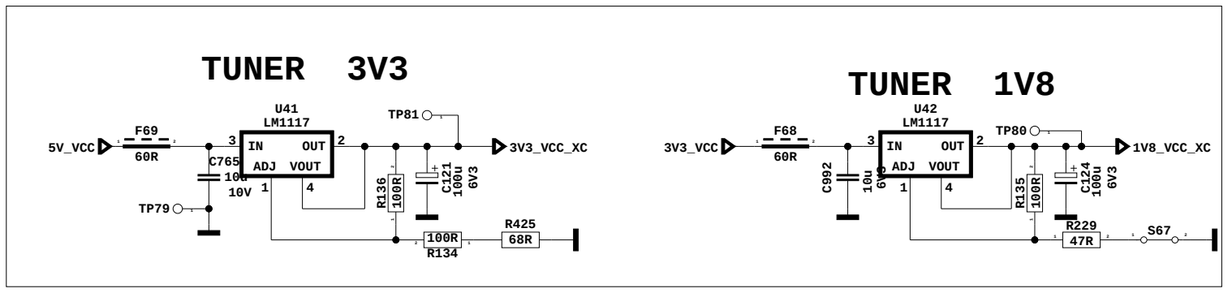










| | | |
|---|---|---|
| VESTEL | PROJECT NAME : 17MB65 | A3 |
| SCH NAME :<DRAWING NAME HERE> | SHEET: | OF:15 |
| DRAWN BY :<YOUR NAME HERE> | 03-11-2010_08:56 | |

## SCART 1

SC1 — SCART LT1

21 SC_CVBS_IN — C805 33p 50V
20 SC_CVBS_OUT — C807 50V 33p
18 — R400 75R — C808 50V 33p — R230 47R — SC_FB
16 — R405 75R — C804 50V 33p — SC_R
15 — R406 75R — R401 75R — UART-TX-SC
13 — C806 50V 33p — SC_G
12 — R399 75R — UART-RX-SC
10 — R407 75R — R396 4k7 — SC_PIN8 — R394 1k2
9 — D15 C15V — C702 100n 10V
8 — SC_B
7 — C803 50V 33p
6 — C827 330p 50V — SCART_AUD_L_IN
5 — F32 600R — R147 100R — SC_AUD_L_OUT
4 — C793 4n7 50V
3 — SCART_AUD_R_IN
2 — C828 330p 50V — F31 600R — R148 100R — SC_AUD_R_OUT
1 — C792 4n7 50V

SC_CVBS_IN — SCART_AUD_L_IN — SCART_AUD_R_IN — JK2: 4 YEL, 3 WHT, 2 RED, 1

D4, D5: NUP4604M5

**INDIA OPTION**

## S-VIDEO IN

SVHS_C_IN — TP83 — 75R R415 — C844 56V 220p — D16 C5V6 — JK6 — TP85 — D17 C5V6 — C843 56V 220p — R418 75R — TP82 — SVHS_Y_IN

## SCART VIDEO OUTPUT AMPLIFIER

12V_VCC — R419 220R — F11 330R — C854 10u 16V — C856 10u 16V
BC858B Q34: R440 390R, R475 68R
Q11 BC848B: C855 10u 10V — CVBS0_OUT
SC_CVBS_OUT — R416 68R — R431 300R
R457 33k — C809 100p 50V — R110 100R — R458 33k

12V_VCC — R420 220R — F12 330R — C857 10u 16V — C859 10u 16V
BC858B Q35: R441 390R, R476 68R
Q10 BC848B: C860 10u 10V — CVBS0_OUT
SC2_CVBS_OUT — R417 68R — R432 300R
R459 33k — C810 100p 50V — R427 100R — R460 33k

## SCART 2

SC2 — SCART LT1

21 SC2_CVBS_IN — C801 33p 50V — S72 S73 — UART-TX-SC, UART-RX-SC
20 SC2_CVBS_OUT
19 — S10 — LED3 — C800 50V 33p
17 — S71 S26 — UART-TX-SC, UART-RX-SC
16 SVHS_C_IN — R397 75R — C802 50V 33p
14 — R395 4k7 — SC2_PIN8 — R393 1k2
13 — D14 C15V — C701 100n 10V
9 SCART2_AUD_L_IN
8 — C825 330p 50V — C790 4n7 50V — F30 600R — R145 100R — SC2_AUD_L_OUT
7 SCART2_AUD_R_IN
6 — F29 600R — R144 100R — SC2_AUD_R_OUT — C824 330p 50V — C791 4n7 50V

D9: NUP4604M5

C782 470p 50V — R385 12k — R319 10k — SCART_AUD_L_IN — SC_AUD_L_IN
SCART_AUD_R_IN — R320 10k — SC_AUD_R_IN — R386 12k
C783 470p 50V
C779 470p 50V — R382 12k — R315 10k — SCART2_AUD_L_IN — SCART2_AUD_LIN
SCART2_AUD_R_IN — R314 10k — SCART2_AUD_RIN — R381 12k
C778 470p 50V

SC2_AUD_L_OUT — R151 100R — SC_AUD_L_OUT
SC2_AUD_R_OUT — R146 100R — SC_AUD_R_OUT

## SC2 INDIA OPTION

SC2_CVBS_IN — JK1: 4 YEL, 3 WHT, 2 RED, 1 — SCART2_AUD_L_IN, SCART2_AUD_R_IN

## DEBUG

5V_STBY — S75 — CN7: 1, 2, 3, 4
UART-RX-SC — R402 75R
UART-TX-SC — R403 75R

## SPDIF OUT

C884 22p 50V — S61 — SPDIF_COAX — JK11: 2, 3, 1 — S80
IR1: VIN 3, VCC 2, GND 1
CN8: 1, 2 — 5V_SPDIF
D19 C5V6 — C704 100n 10V
S167
5V_SPDIF — F25 600R — 5V_VCC
C886 22p 50V — C885 22p 50V
R42 4k7 — C932 100n 10V — R150 100R — SPDIF_OUT
Q9 BC848B
C931 100n 10V — SPDIF_COAX — R354 220R — R41 4k7
R190 220R

## YPBPR&SUBW AUDIO

S137 — 50V 330p C830 — R389 12k — C784 470p 50V — R388 12k
WHT 1 2 — 10k R321 — YPbPr1LEFT
RED 3 4 — 10k R322 — YPbPr1RIGHT
BLK 5 6 — JK3 — C833 330p 50V — R390 12k — 12k R387 50V 470p — C785
F13 600R — 100R R109 50V 1n — C12 — C29 22u 16V — SUBW_OUT

## VGA CONNECTOR

CN6: 15 VGA-TX, 14 VGA_DDC_5V, 13 VGA-RX
D6: NUP4604M5
R316 10k, R317 10k, R318 10k
TP84 — 5V_VCC — D29 BAV70 — VGA_DDC_5V — C703 100n 10V
U3 ST24LC21: VCC A0 8, WP A1 7, SCL A2 6, SDA GND 5
R481 100R — R1 8, R2 7, R3 6, R4 5
2k2 R479, 2k2 R480
TP88 TP87 TP86 TP89
R149 100R — VGA_HSNC
VGA_VSNC
S79 — UART-RX-SC
S78 — UART-TX-SC
VGA-RX — NC S76
VGA-TX — NC S77
C874 27p 50V — C875 27p 50V — C873 27p 50V
VGA_B, VGA_G, VGA_R
R412 75R — R413 75R — R414 75R
D7: NUP4604M5

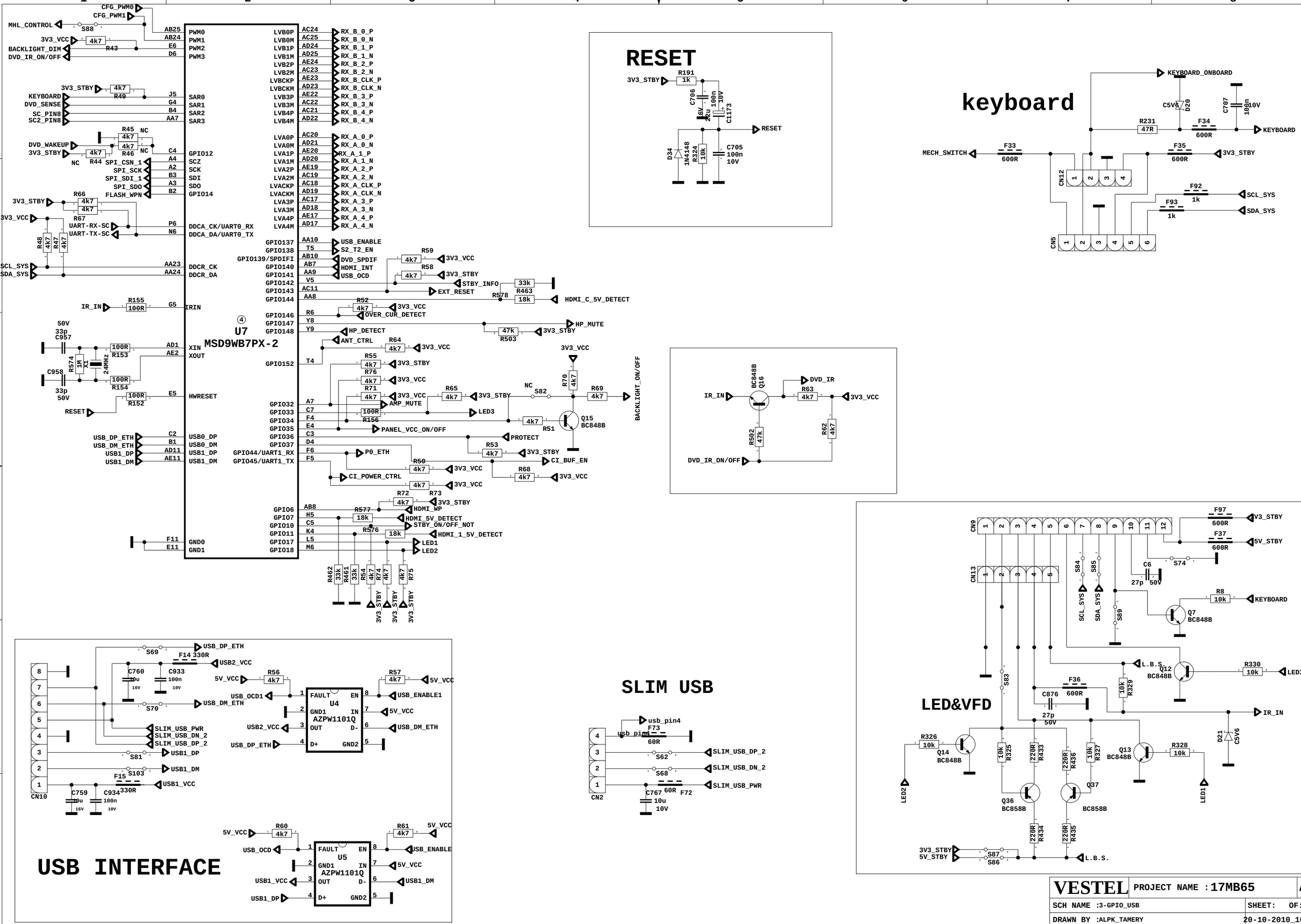
## YPBPR INPUT

D8: NUP4604M5
50V NC 27p — C870
JK4: RED 6 5, BLU 4 3, GRN 2 1
75R R410 — YPbPr_PR
75R R411 — YPbPr_PB
YPbPr_Y
R409 75R — C871 27p 50V NC
50V 27p NC — C872

## SIDE AV INPUT

SLIM_SAV_AUD_L_IN — C826 330p 50V — F26 600R — SAV_AUD_R_IN
SLIM_SAV_AUD_R_IN — C829 330p 50V — F27 600R — SAV_AUD_L_IN
JK5: RED 6 5, WHT 4 3, YLW 2 1
F28 600R — SAV_CVBS
D18 C5V6 — C842 220p 50V — R408 75R
usb_pin4
C780 470p 50V — R383 12k — SAV_L_IN
R323 10k — R423 1k2 — SAV_R_IN
R384 12k 50V 470p — C781

| | | |
|---|---|---|
| VESTEL | PROJECT NAME :17MB65 | A3 |
| SCH NAME :2-VIDEO_AUDIO | SHEET: | OF:15 |
| DRAWN BY :ALPK_TAMERY | 02-11-2010_13:30 | |


MSD9WB7PX-2
U7
RESET
keyboard
SLIM USB
LED&VFD
USB INTERFACE
U4
AZPW1101Q
U5
AZPW1101Q
VESTEL
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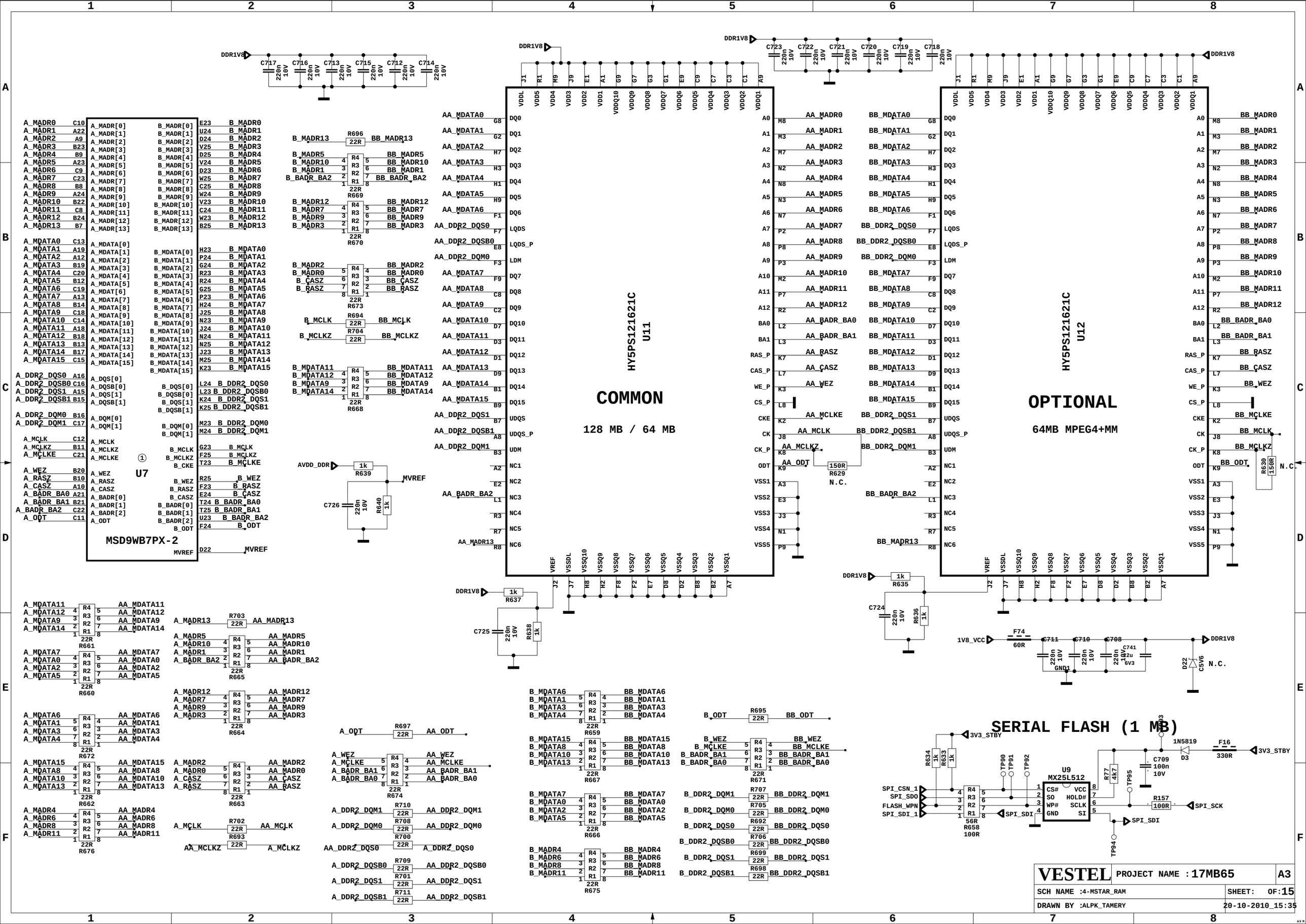
A3
SCH NAME :3-GPIO_USB
SHEET: OF:15
DRAWN BY :ALPK_TAMERY
20-10-2010_10:57


DDR1V8
C717 220n 10V
C716 220n 10V
C713 220n 10V
C715 220n 10V
C712 220n 10V
C714 220n 10V
C723 220n 10V
C722 220n 10V
C721 220n 10V
C720 220n 10V
C719 220n 10V
C718 220n 10V
U7
MSD9WB7PX-2
HY5PS121621C U11
COMMON
128 MB / 64 MB
HY5PS121621C U12
OPTIONAL
64MB MPEG4+MM
SERIAL FLASH (1 MB)
U9 MX25L512
VESTEL
PROJECT NAME :17MB65
A3
SCH NAME :4-MSTAR_RAM
SHEET: OF:15
DRAWN BY :ALPK_TAMERY
20-10-2010_15:35

# AUDIO OUTPUTs

## MODE SELECTION

1: NAND
0: IPS

| | |
|---|---|
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| SCH NAME :5-SUPPLY_INPUTS | SHEET: OF:15 |
| DRAWN BY :ALPK_TAMERY | 25-10-2010_16:40 |

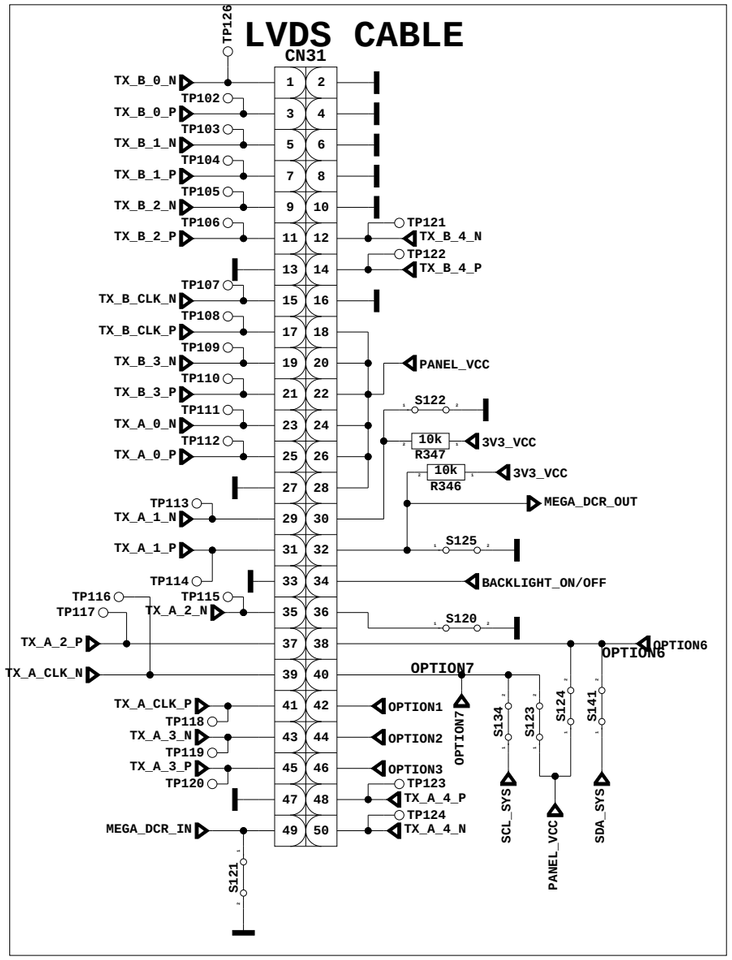
# CI INTERFACE

# NAND FLASH (64 MB)

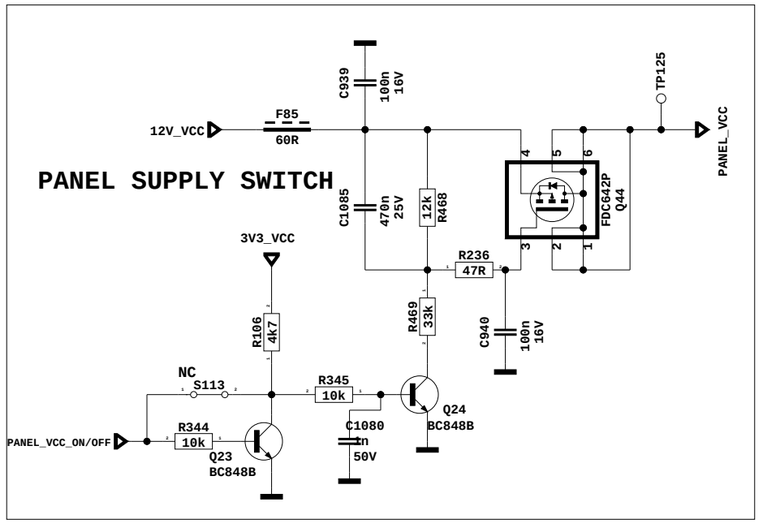
Ethernet lines must be 100ohm differential pairs

| | |
|---|---|
| VESTEL | PROJECT NAME :17MB65 |
| | A3 |
| SCH NAME :6-CI_ETHERNET | SHEET: OF:15 |
| DRAWN BY :ALPK_TAMERY | 04-11-2010_15:55 |

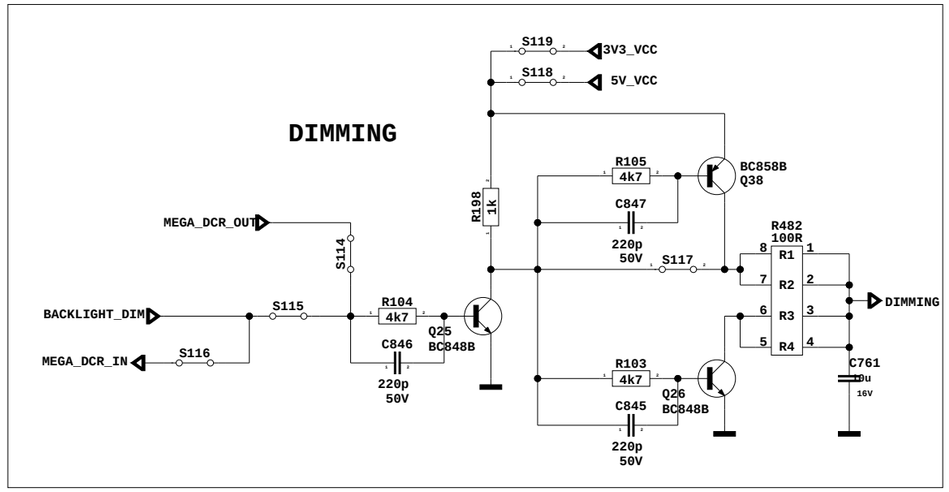
# LVDS CABLE



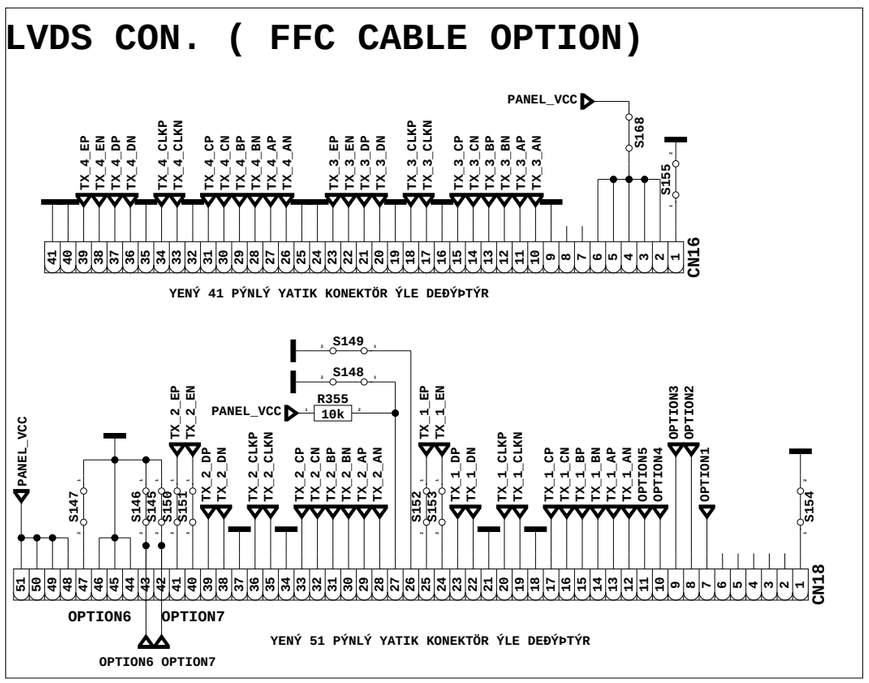

# PANEL SUPPLY SWITCH



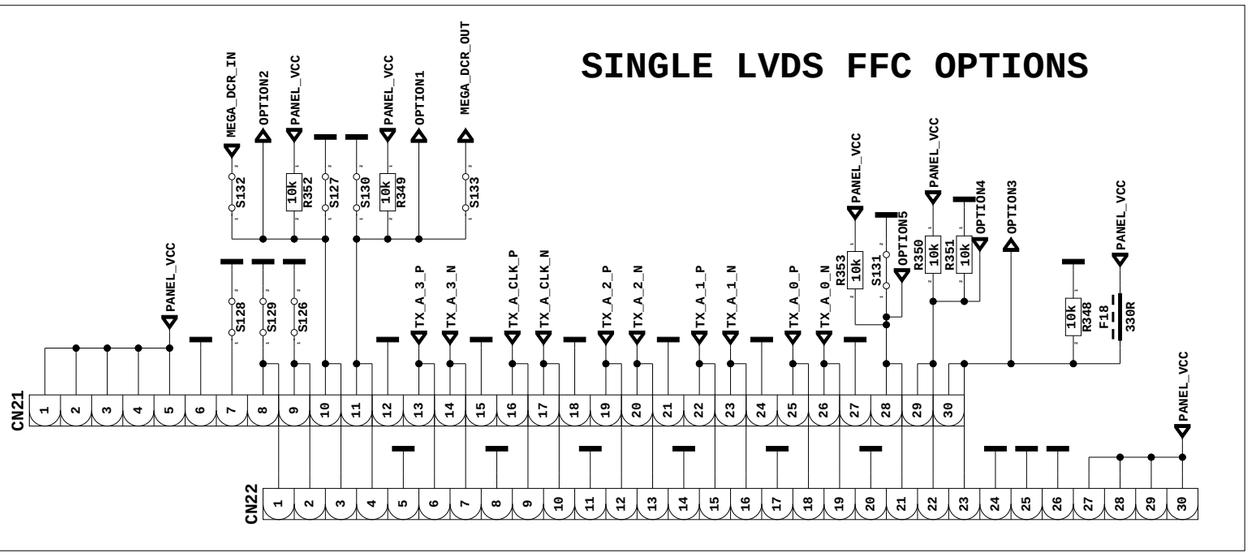

# DIMMING




# LVDS CON. ( FFC CABLE OPTION)




# SINGLE LVDS FFC OPTIONS

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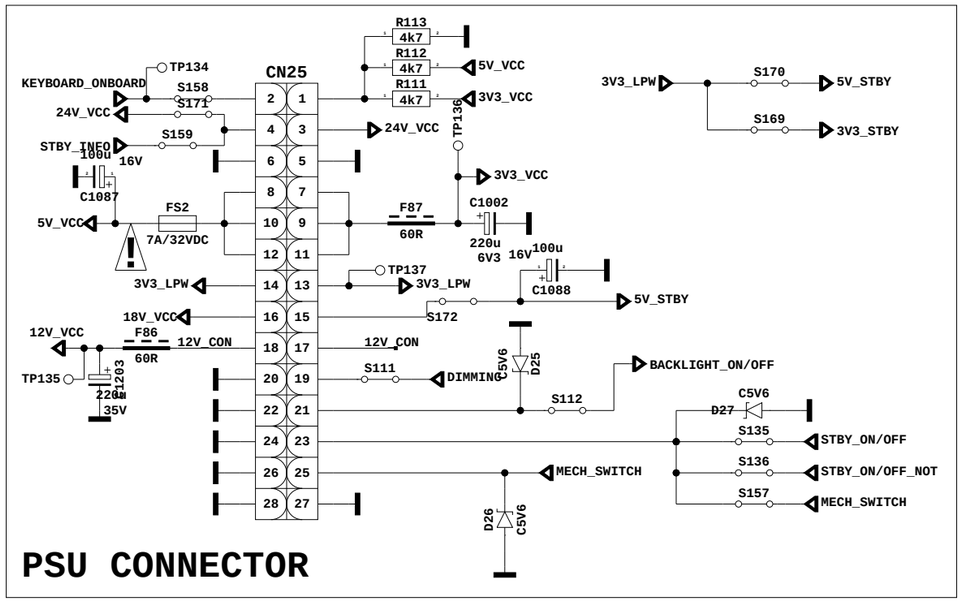
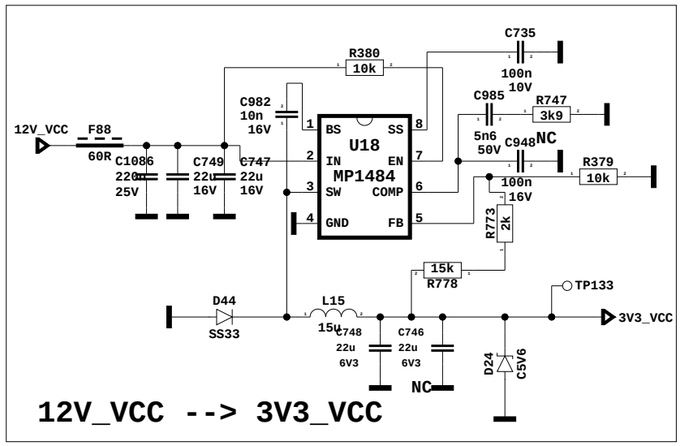
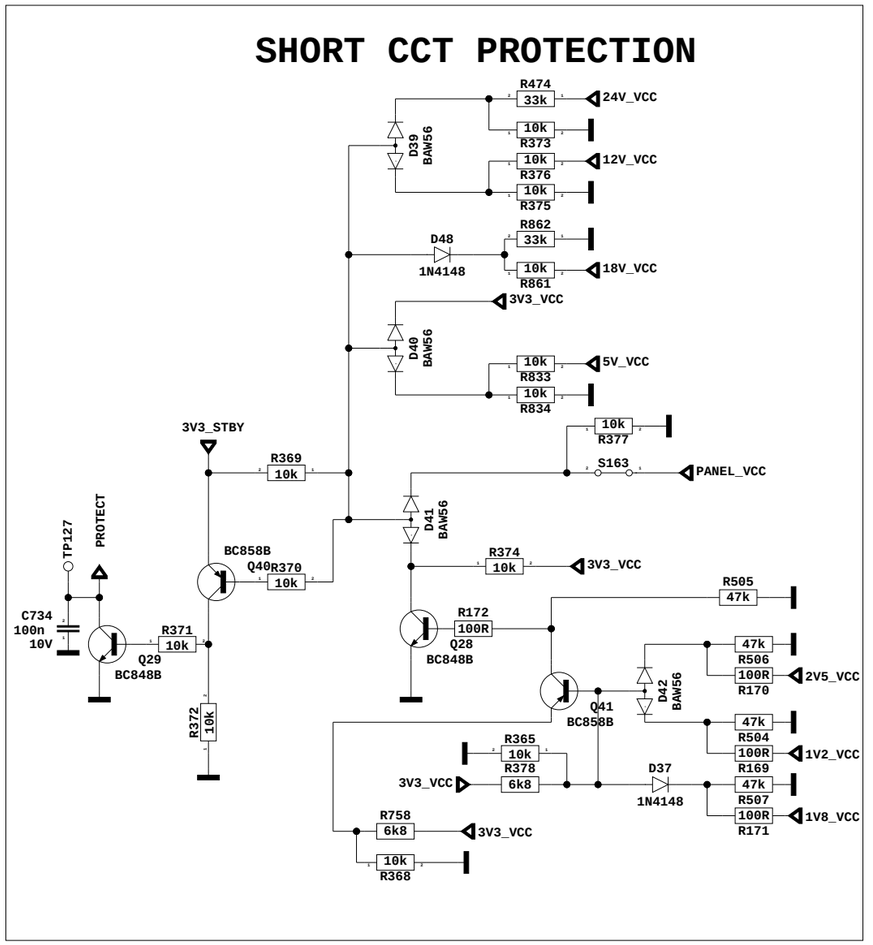
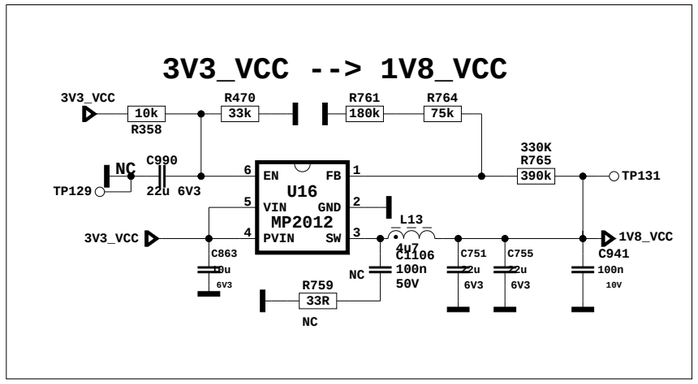
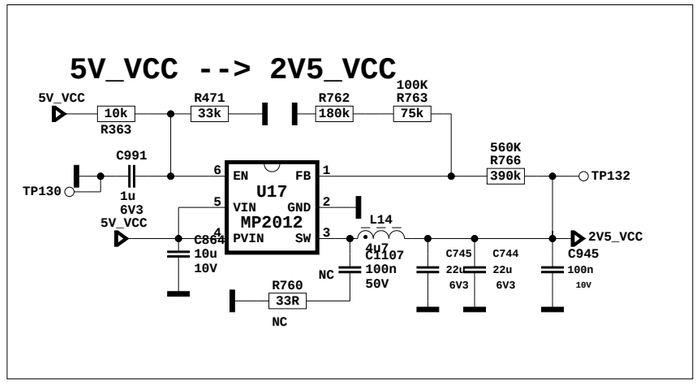
| SCH NAME : LVDS_CONNECTOR | SHEET: | OF: 15 |
| DRAWN BY : ALPK_TAMERY | 23-07-2010_14:18 | |

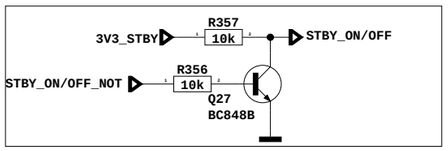


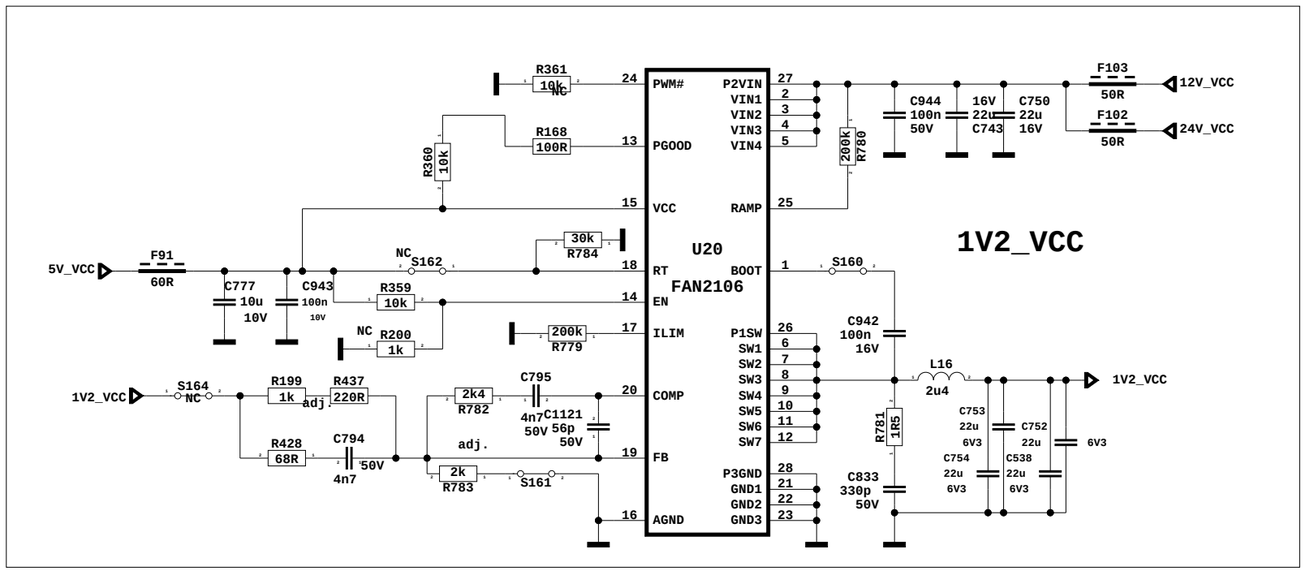



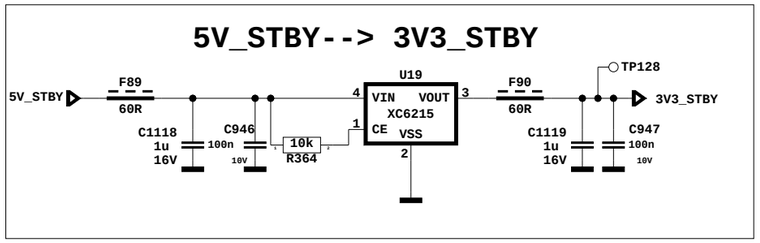

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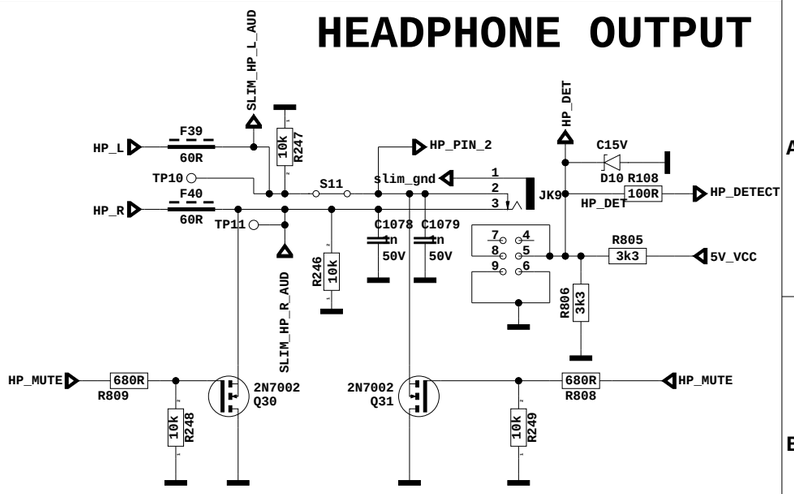
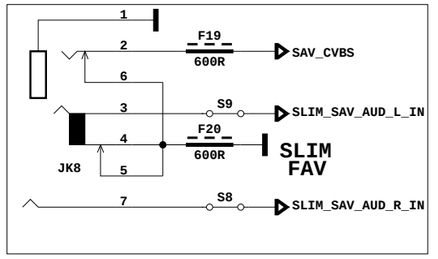
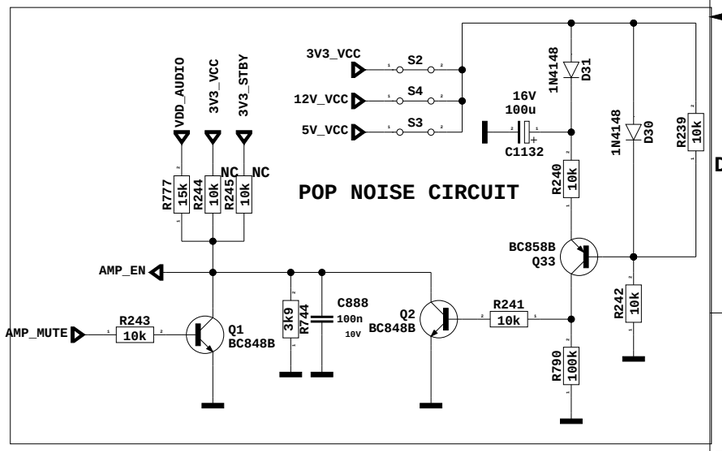
| DRAWN BY :ALPK_TAMERY | 04-11-2010_11:31 | |

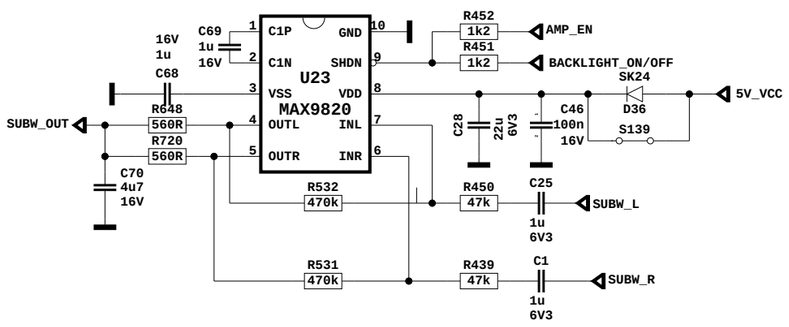
# HEADPHONE OUTPUT

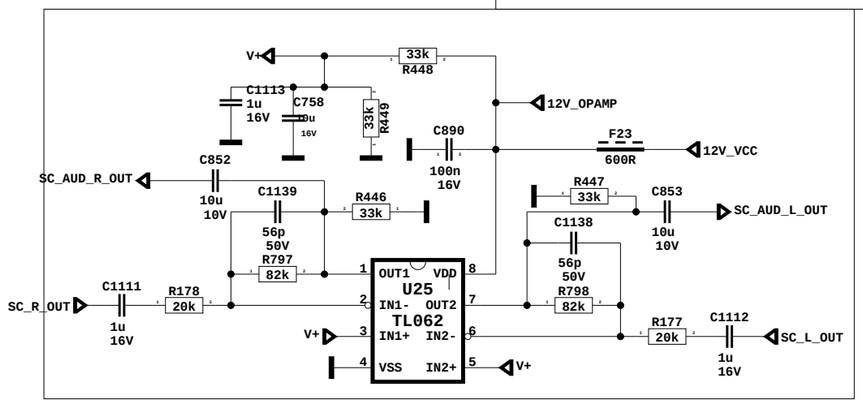


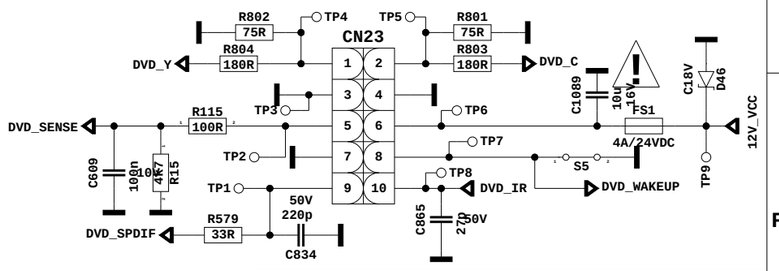








## DVD INTERFACE (for 26" to 32")




| | | |
|---|---|---|
| VESTEL | PROJECT NAME :17MB65 | A3 |
| SCH NAME :9-SUB_WFR/OUTPUTS | SHEET: | OF:15 |
| DRAWN BY :ALPK_TAMERY | 04-11-2010_11:36 | |

# T2 DEMOD

U32
CXD2820R

FILTER COMPONENTS WILL DEPEND ON TUNER TYPE USED

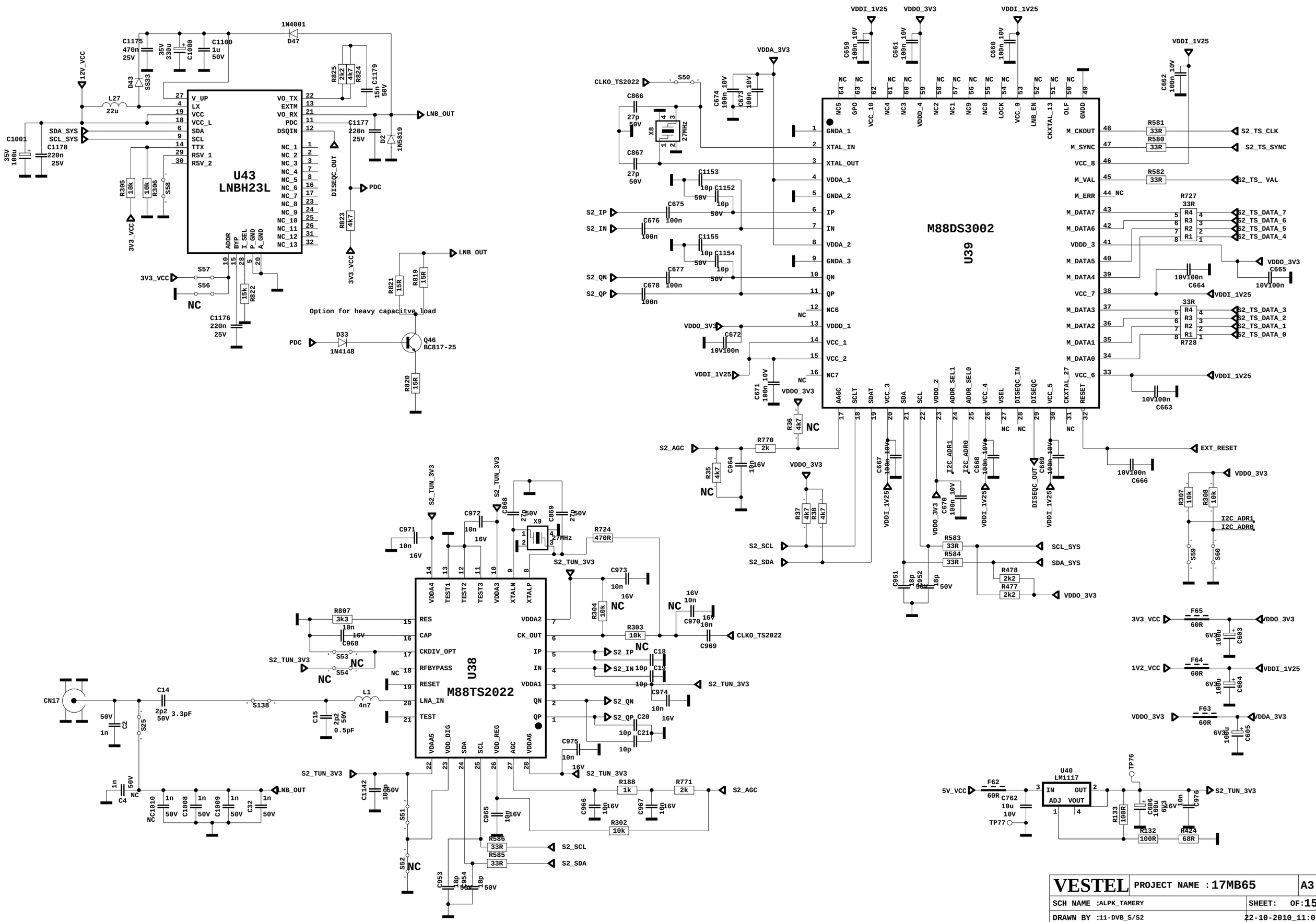
## T2 BUFFER BYPASS

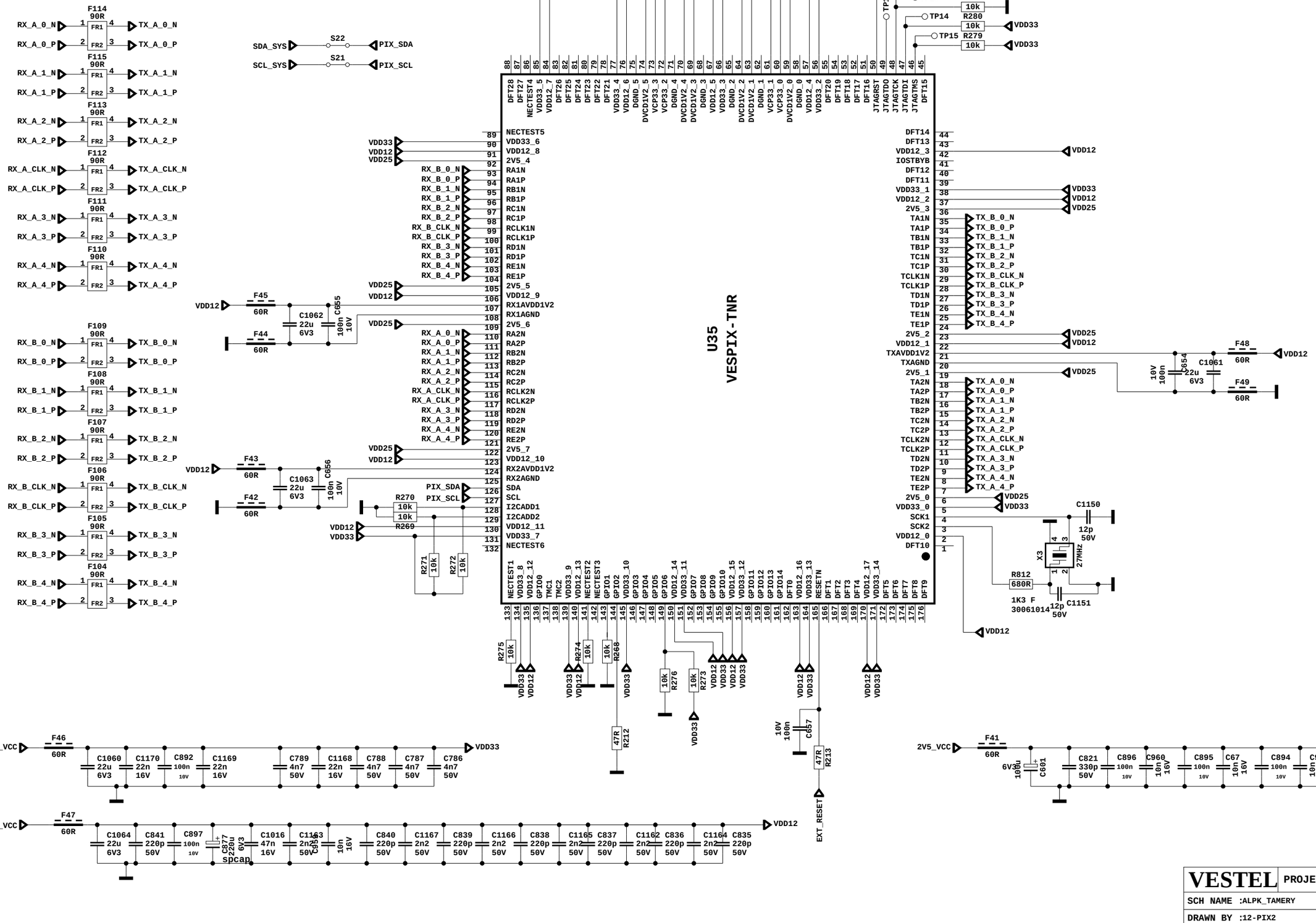
## T2 S2 BUFFER

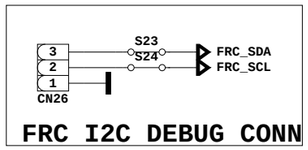
## CI BUFFER

## CI BUFFER BYPASS

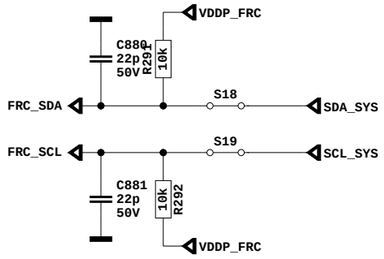
| | | |
|---|---|---|
| VESTEL | PROJECT NAME : 17MB65 | A3 |
| SCH NAME : ALPK_TAMERY | SHEET: | OF:15 |
| DRAWN BY : 10-T2_DEMOD | 20-10-2010_15:32 | |

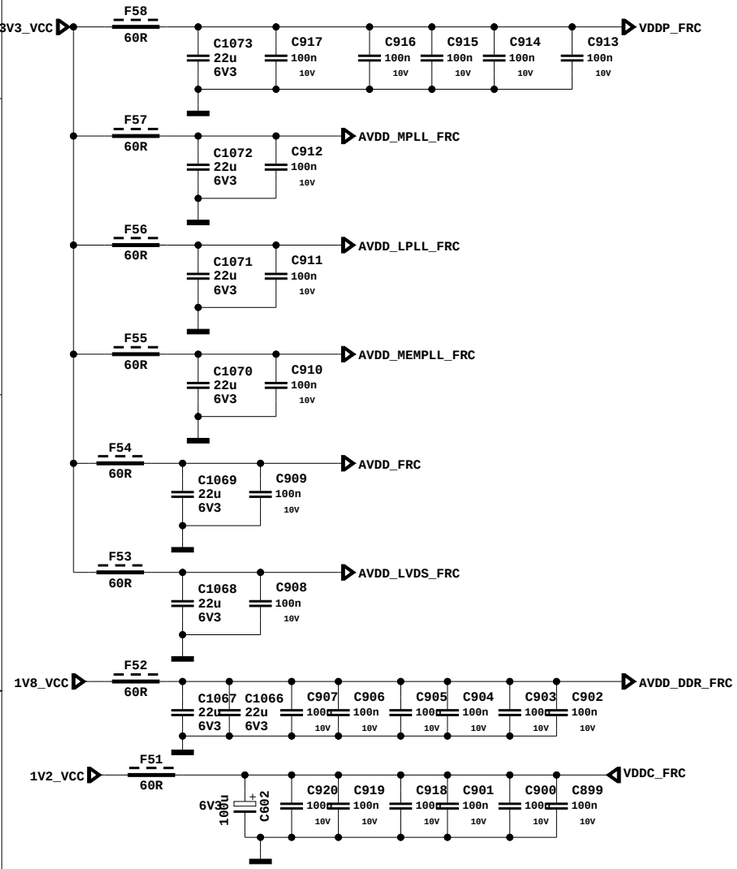

U43
LNBH23L
V_UP
LX
VCC
VCC_L
SDA
SCL
TTX
RSV_1
RSV_2
VO_TX
EXTM
VO_RX
PDC
DSQIN
NC_1
NC_2
NC_3
NC_4
NC_5
NC_6
NC_7
NC_8
NC_9
NC_10
NC_11
NC_12
NC_13
ADDR
BYP
I_SEL
P_GND
A_GND
12V_VCC
SDA_SYS
SCL_SYS
3V3_VCC
LNB_OUT
PDC
DISEQC_OUT
Option for heavy capacitive load
NC
1N4001
D47
1N4148
D33
1N5819
D2
Q46
BC817-25
M88DS3002
U39
VDDI_1V25
VDDO_3V3
VDDA_3V3
CLKO_TS2022
EXT_RESET
S2_TS_CLK
S2_TS_SYNC
S2_TS_ VAL
S2_TS_DATA_7
S2_TS_DATA_6
S2_TS_DATA_5
S2_TS_DATA_4
S2_TS_DATA_3
S2_TS_DATA_2
S2_TS_DATA_1
S2_TS_DATA_0
S2_IP
S2_IN
S2_QN
S2_QP
S2_AGC
S2_SCL
S2_SDA
SCL_SYS
SDA_SYS
I2C_ADR1
I2C_ADR0
M88TS2022
U38
S2_TUN_3V3
CN17
LNB_OUT
U40
LM1117
5V_VCC
VESTEL
PROJECT NAME :17MB65
A3
SCH NAME :ALPK_TAMERY
SHEET: OF:15
DRAWN BY :11-DVB_S/S2
22-10-2010_11:07

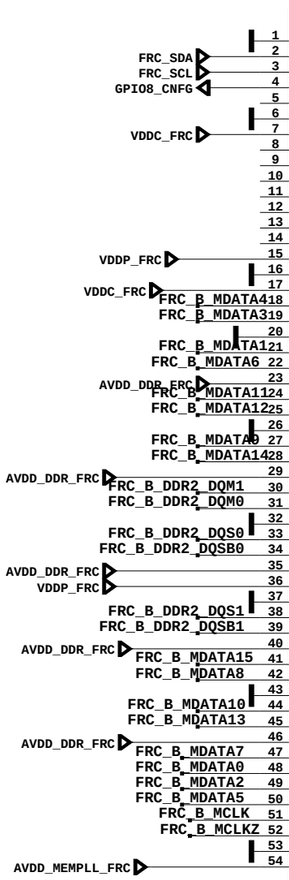

U35
VESPIX-TNR
F114 90R
F115 90R
F113 90R
F112 90R
F111 90R
F110 90R
F109 90R
F108 90R
F107 90R
F106 90R
F105 90R
F104 90R
RX_A_0_N
RX_A_0_P
RX_A_1_N
RX_A_1_P
RX_A_2_N
RX_A_2_P
RX_A_CLK_N
RX_A_CLK_P
RX_A_3_N
RX_A_3_P
RX_A_4_N
RX_A_4_P
RX_B_0_N
RX_B_0_P
RX_B_1_N
RX_B_1_P
RX_B_2_N
RX_B_2_P
RX_B_CLK_N
RX_B_CLK_P
RX_B_3_N
RX_B_3_P
RX_B_4_N
RX_B_4_P
TX_A_0_N
TX_A_0_P
TX_A_1_N
TX_A_1_P
TX_A_2_N
TX_A_2_P
TX_A_CLK_N
TX_A_CLK_P
TX_A_3_N
TX_A_3_P
TX_A_4_N
TX_A_4_P
TX_B_0_N
TX_B_0_P
TX_B_1_N
TX_B_1_P
TX_B_2_N
TX_B_2_P
TX_B_CLK_N
TX_B_CLK_P
TX_B_3_N
TX_B_3_P
TX_B_4_N
TX_B_4_P
SDA_SYS
SCL_SYS
S22
S21
PIX_SDA
PIX_SCL
TP16
TP17
TP13
TP14
TP15
R277 10k
R278 10k
R280 10k
R279 10k
VDD33
F45 60R
F44 60R
F43 60R
F42 60R
C1062 22u 6V3
C655 100n 10V
C1063 22u 6V3
C656 100n 10V
R270 10k
R269 10k
R271 10k
R272 10k
F48 60R
F49 60R
C654 10V 100n
C1061 22u 6V3
C1150 12p 50V
C1151 12p 50V
X3 27MHz
R812 680R
1K3 F 30061014
R275 10k
R274 10k
R268 10k
R276 10k
R273 10k
47R R212
47R R213
C657 10V 100n
EXT_RESET
F46 60R
F47 60R
F41 60R
3V3_VCC
1V2_VCC
2V5_VCC
C1060 22u 6V3
C1170 22n 16V
C892 100n 10V
C1169 22n 16V
C789 4n7 50V
C1168 22n 16V
C788 4n7 50V
C787 4n7 50V
C786 4n7 50V
C1064 22u 6V3
C841 220p 50V
C897 100n 10V
C877 220u 6V3
spcap
C1016 47n 16V
C1163 2n2 50V
C695 10n 16V
C840 220p 50V
C1167 2n2 50V
C839 220p 50V
C1166 2n2 50V
C838 220p 50V
C1165 2n2 50V
C837 220p 50V
C1162 2n2 50V
C836 220p 50V
C1164 2n2 50V
C835 220p 50V
C601 100u 6V3
C821 330p 50V
C896 100n 10V
C960 10n 16V
C895 100n 10V
C67 10n 16V
C894 100n 10V
C962 10n 16V
C893 100n 10V
C963 10n 16V
VESTEL
PROJECT NAME :17MB65
A3
SCH NAME :ALPK_TAMERY
SHEET: OF:15
DRAWN BY :12-PIX2
21-10-2010_17:01




## FRC I2C DEBUG CONN.

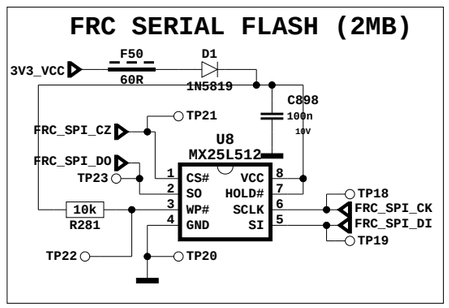


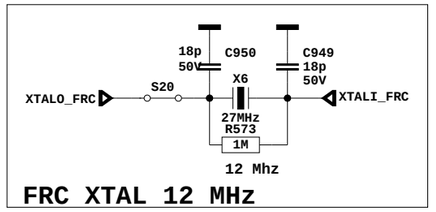



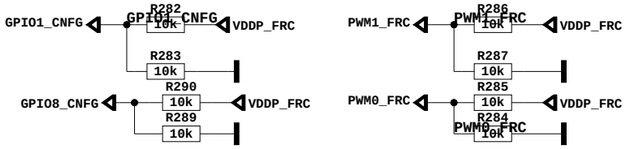










| | | |
|---|---|---|
| VESTEL | PROJECT NAME :17MB65 | A3 |
| SCH NAME :ALPK_TAMERY | SHEET: | OF:15 |
| DRAWN BY :13-FRC | 22-07-2010_16:23 | |

TX_3_AP TP47
TX_3_AN TP46
TX_3_BN TP45
TX_3_BP TP44
TX_3_CLKN TP43
TX_3_CLKP TP42
TX_3_CN TP41
TX_3_CP TP40
TX_3_DN TP39
TX_3_DP TP38
TX_3_EN TP37
TX_3_EP TP36
TX_4_AN TP35
TX_4_AP TP34
TX_4_BN TP33
TX_4_BP TP32
TX_4_CLKN TP31
TX_4_CLKP TP30
TX_4_CN TP28
TX_4_CP TP29
TX_4_DN TP27
TX_4_DP TP26
TX_4_EN TP25
TX_4_EP TP24

TX_1_AP TP71
TX_1_AN TP70
TX_1_BN TP69
TX_1_BP TP68
TX_1_CLKN TP67
TX_1_CLKP TP66
TX_1_CN TP65
TX_1_CP TP64
TX_1_DN TP63
TX_1_DP TP62
TX_1_EN TP61
TX_1_EP TP60
TX_2_AN TP59
TX_2_AP TP58
TX_2_BN TP57
TX_2_BP TP56
TX_2_CLKP TP55
TX_2_CLKN TP54
TX_2_CN TP52
TX_2_CP TP53
TX_2_DN TP51
TX_2_DP TP50
TX_2_EN TP49
TX_2_EP TP48

F137 90R: TX_A_0_N ↔ TX_A_0_N_FRC; TX_A_0_P ↔ TX_A_0_P_FRC
F138 90R: TX_A_1_N ↔ TX_A_1_N_FRC; TX_A_1_P ↔ TX_A_1_P_FRC
F136 90R: TX_A_2_N ↔ TX_A_2_N_FRC; TX_A_2_P ↔ TX_A_2_P_FRC
F135 90R: TX_A_3_N ↔ TX_A_3_N_FRC; TX_A_3_P ↔ TX_A_3_P_FRC
F134 90R: TX_A_4_N ↔ TX_A_4_N_FRC; TX_A_4_P ↔ TX_A_4_P_FRC
F133 90R: TX_A_CLK_N ↔ TX_A_CLK_N_FRC; TX_A_CLK_P ↔ TX_A_CLK_P_FRC

F132 90R: TX_B_0_N ↔ TX_B_0_N_FRC; TX_B_0_P ↔ TX_B_0_P_FRC
F131 90R: TX_B_1_N ↔ TX_B_1_N_FRC; TX_B_1_P ↔ TX_B_1_P_FRC
F130 90R: TX_B_2_N ↔ TX_B_2_N_FRC; TX_B_2_P ↔ TX_B_2_P_FRC
F129 90R: TX_B_3_N ↔ TX_B_3_N_FRC; TX_B_3_P ↔ TX_B_3_P_FRC
F128 90R: TX_B_4_N ↔ TX_B_4_N_FRC; TX_B_4_P ↔ TX_B_4_P_FRC
F127 90R: TX_B_CLK_N ↔ TX_B_CLK_N_FRC; TX_B_CLK_P ↔ TX_B_CLK_P_FRC

FRC_DDR18V

HY5PS121621C U10

64 MB

| | | | |
|---|---|---|---|
| VDDL J1 | VDD5 R1 | VDD4 M9 | VDD3 J9 |
| VDD2 E1 | VDD1 A1 | VDDQ10 G9 | VDDQ9 C7 |
| VDDQ8 G3 | VDDQ7 G1 | VDDQ6 E9 | VDDQ5 C9 |
| VDDQ4 C7 | VDDQ3 C3 | VDDQ2 C1 | VDDQ1 A9 |

| | | | |
|---|---|---|---|
| DQ0 G8 | DQ1 G2 | DQ2 H7 | DQ3 H3 |
| DQ4 H1 | DQ5 H9 | DQ6 F1 | LQDS F7 |
| LQDS_P E8 | LDM F3 | DQ7 F9 | DQ8 C8 |
| DQ9 C2 | DQ10 D7 | DQ11 D3 | DQ12 D1 |
| DQ13 D9 | DQ14 B1 | DQ15 B9 | UDQS B7 |
| UDQS_P A8 | UDM B3 | NC1 A2 | NC2 E2 |
| NC3 L1 | NC4 R3 | NC5 R7 | NC6 R8 |

| | | | |
|---|---|---|---|
| A0 M8 | A1 M3 | A2 M7 | A3 N2 |
| A4 N8 | A5 N3 | A6 N7 | A7 P2 |
| A8 P8 | A9 P3 | A10 M2 | A11 P7 |
| A12 R2 | BA0 L2 | BA1 L3 | RAS_P K7 |
| CAS_P L7 | WE_P K3 | CS_P L8 | CKE K2 |
| CK J8 | CK_P K8 | ODT K9 | VSS1 A3 |
| VSS2 E3 | VSS3 J3 | VSS4 N1 | VSS5 P9 |

| | | | |
|---|---|---|---|
| VREF J2 | VSSDL J7 | VSSQ10 H8 | VSSQ9 H2 |
| VSSQ8 F8 | VSSQ7 F2 | VSSQ6 E7 | VSSQ5 D8 |
| VSSQ4 D2 | VSSQ3 B8 | VSSQ2 B2 | VSSQ1 A7 |

FRC_BB_MDATA0 FRC_BB_MDATA1 FRC_BB_MDATA2 FRC_BB_MDATA3 FRC_BB_MDATA4 FRC_BB_MDATA5 FRC_BB_MDATA6 FRC_BB_DDR2_DQS0 FRC_BB_DDR2_DQSB0 FRC_BB_DDR2_DQM0 FRC_BB_MDATA7 FRC_BB_MDATA8 FRC_BB_MDATA9 FRC_BB_MDATA10 FRC_BB_MDATA11 FRC_BB_MDATA12 FRC_BB_MDATA13 FRC_BB_MDATA14 FRC_BB_MDATA15 FRC_BB_DDR2_DQS1 FRC_BB_DDR2_DQSB1 FRC_BB_DDR2_DQM1

FRC_BB_MADR0 FRC_BB_MADR1 FRC_BB_MADR2 FRC_BB_MADR3 FRC_BB_MADR4 FRC_BB_MADR5 FRC_BB_MADR6 FRC_BB_MADR7 FRC_BB_MADR8 FRC_BB_MADR9 FRC_BB_MADR10 FRC_BB_MADR11 FRC_BB_MADR12 FRC_BB_BADR_BA0 FRC_BB_BADR_BA1 FRC_BB_RASZ FRC_BB_CASZ FRC_BB_WEZ FRC_BB_MCLKE FRC_BB_MCLK FRC_BB_MCLKZ FRC_BB_ODT GND1

R294 nc 10k; R293 nc 10k (FRC_DDR18V)

C822 330p 50V; C921 100n 10V; R632 1k; R631 1k

1V8_VCC — F59 60R — FRC_DDR18V

C1074 22u 6V3; C823 330p 50V; C922 100n 10V; C878 6V3 220u spcap

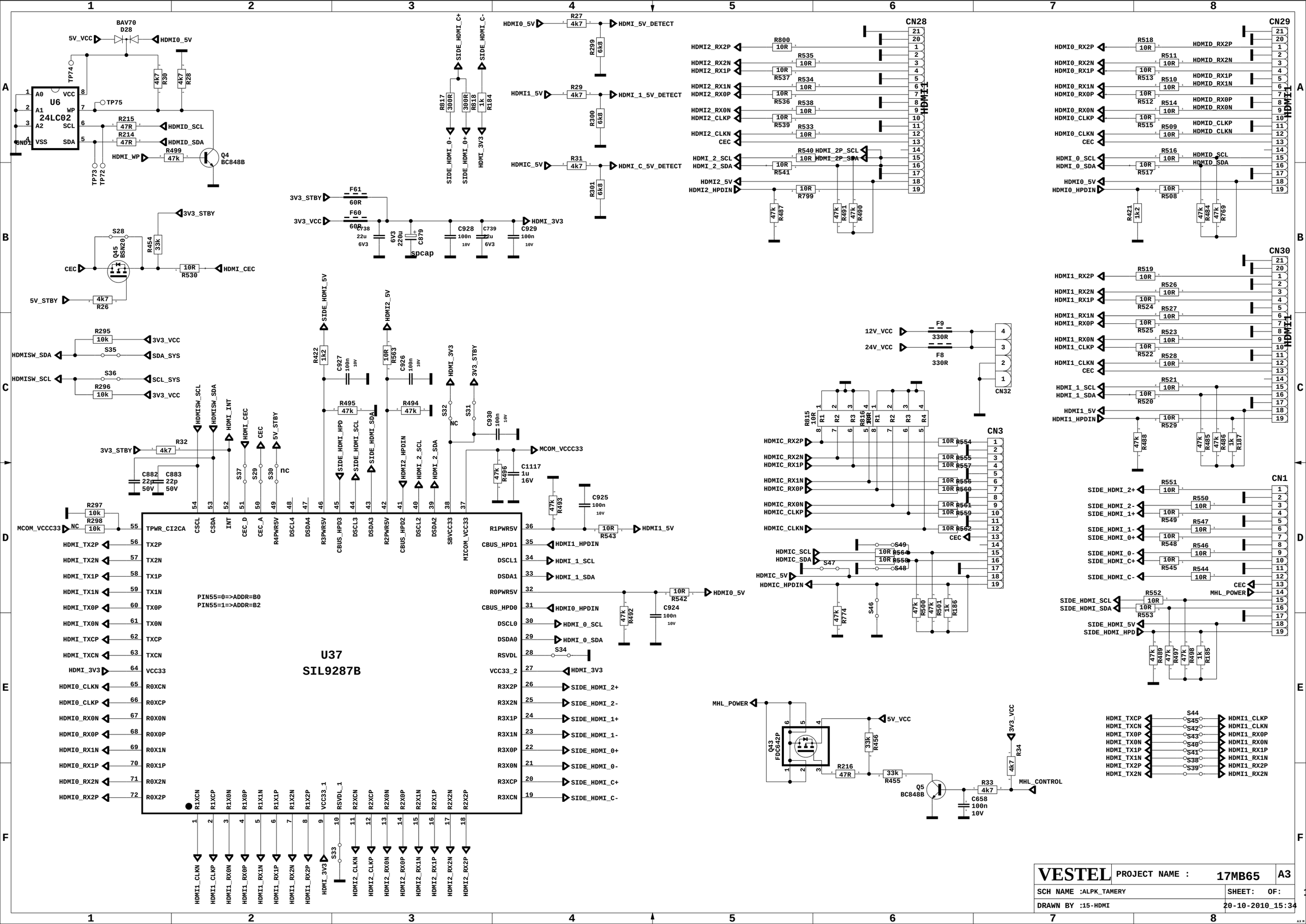
TX_B_0_N_FRC TX_B_0_P_FRC → F139 90R → TX_1_AN TX_1_AP
TX_B_1_N_FRC TX_B_1_P_FRC → F126 90R → TX_1_BN TX_1_BP
TX_B_2_N_FRC TX_B_2_P_FRC → F125 90R → TX_1_CN TX_1_CP
TX_B_CLK_N_FRC TX_B_CLK_P_FRC → F124 90R → TX_1_CLKN TX_1_CLKP
TX_B_3_N_FRC TX_B_3_P_FRC → F123 90R → TX_1_DN TX_1_DP
TX_B_4_N_FRC TX_B_4_P_FRC → F122 90R → TX_1_EN TX_1_EP

TX_A_0_N_FRC TX_A_0_P_FRC → F121 90R → TX_2_AN TX_2_AP
TX_A_1_N_FRC TX_A_1_P_FRC → F120 90R → TX_2_BN TX_2_BP
TX_A_2_N_FRC TX_A_2_P_FRC → F119 90R → TX_2_CN TX_2_CP
TX_A_CLK_N_FRC TX_A_CLK_P_FRC → F118 90R → TX_2_CLKN TX_2_CLKP
TX_A_3_N_FRC TX_A_3_P_FRC → F117 90R → TX_2_DN TX_2_DP
TX_A_4_N_FRC TX_A_4_P_FRC → F116 90R → TX_2_EN TX_2_EP

R120 100R: TX_A_0_N_FRC TX_A_0_P_FRC
R121 100R: TX_A_1_N_FRC TX_A_1_P_FRC
R122 100R: TX_A_2_N_FRC TX_A_2_P_FRC
R123 100R: TX_A_3_N_FRC TX_A_3_P_FRC
R124 100R: TX_A_4_N_FRC TX_A_4_P_FRC
R125 100R: TX_A_CLK_N_FRC TX_A_CLK_P_FRC

R127 100R: TX_B_0_N_FRC TX_B_0_P_FRC
R128 100R: TX_B_1_N_FRC TX_B_1_P_FRC
R129 100R: TX_B_2_N_FRC TX_B_2_P_FRC
R130 100R: TX_B_3_N_FRC TX_B_3_P_FRC
R126 100R: TX_B_4_N_FRC TX_B_4_P_FRC
R131 100R: TX_B_CLK_N_FRC TX_B_CLK_P_FRC

| | | |
|---|---|---|
| VESTEL | PROJECT NAME : 17MB65 | A3 |
| | SCH NAME : ALPK_TAMERY | SHEET: OF: 15 |
| | DRAWN BY : 14-FRC_CON_DDR | 22-07-2010_16:19 |


BAV70
D28
5V_VCC
HDMI0_5V
TP74
4k7 R30
4k7 R28
U6
24LC02
A0
A1
A2
VSS
VCC
WP
SCL
SDA
TP75
R215 47R
R214 47R
HDMID_SCL
HDMID_SDA
HDMI_WP
R499 47k
Q4
BC848B
TP73
TP72
SIDE_HDMI_C+
SIDE_HDMI_C-
R817 300R
R818 300R
R184 1k
SIDE_HDMI_0-
SIDE_HDMI_0+
HDMI_3V3
R27 4k7
R29 4k7
R31 4k7
HDMI0_5V
HDMI1_5V
HDMIC_5V
HDMI_5V_DETECT
HDMI_1_5V_DETECT
HDMI_C_5V_DETECT
R299 6k8
R300 6k8
R301 6k8
CN28
HDMI1
HDMI2_RX2P
HDMI2_RX2N
HDMI2_RX1P
HDMI2_RX1N
HDMI2_RX0P
HDMI2_RX0N
HDMI2_CLKP
HDMI2_CLKN
HDMI2_SCL
HDMI2_SDA
HDMI2_5V
HDMI2_HPDIN
CEC
R800 10R
R535 10R
R537 10R
R534 10R
R536 10R
R538 10R
R539 10R
R533 10R
R540 10R
R541 10R
R799 10R
HDMI_2P_SCL
HDMI_2P_SDA
47k R487
47k R491
47k R490
CN29
HDMI0_RX2P
HDMI0_RX2N
HDMI0_RX1P
HDMI0_RX1N
HDMI0_RX0P
HDMI0_RX0N
HDMI0_CLKP
HDMI0_CLKN
HDMI0_SCL
HDMI0_SDA
HDMI0_5V
HDMI0_HPDIN
CEC
R518 10R
R511 10R
R513 10R
R510 10R
R512 10R
R514 10R
R515 10R
R509 10R
R516 10R
R517 10R
R508 10R
HDMID_RX2P
HDMID_RX2N
HDMID_RX1P
HDMID_RX1N
HDMID_RX0P
HDMID_RX0N
HDMID_CLKP
HDMID_CLKN
HDMID_SCL
HDMID_SDA
R421 1k2
47k R484
47k R769
3V3_STBY
S28
Q45
BSN20
R454 33k
CEC
10R R530
HDMI_CEC
5V_STBY
4k7 R26
F61 60R
F60 60R
3V3_STBY
3V3_VCC
C738 22u 6V3
C879 6V3 220u
spcap
C928 100n 10V
C739 22u 6V3
C929 100n 10V
HDMI_3V3
R295 10k
R296 10k
HDMISW_SDA
HDMISW_SCL
S35
S36
SDA_SYS
SCL_SYS
3V3_VCC
SIDE_HDMI_5V
HDMI2_5V
R422 1k2
R563 10R
C927 100n 10V
C926 100n 10V
R495 47k
R494 47k
HDMI_HPD
HDMI_SCL
HDMI_SDA
HDMI2_HPDIN
HDMI2_SCL
HDMI2_SDA
S32
S31
NC
C930 100n 10V
HDMI_3V3
3V3_STBY
MCOM_VCCC33
C1117 1u 16V
47k R496
47k R493
C925 100n 10V
R32 4k7
3V3_STBY
C882 22p 50V
C883 22p 50V
HDMISW_SCL
HDMISW_SDA
HDMI_INT
HDMI_CEC
CEC
5V_STBY
S37
S29
S30
nc
R297 10k
R298 10k
MCOM_VCCC33
NC
U37
SIL9287B
PIN55=0=>ADDR=B0
PIN55=1=>ADDR=B2
TPWR_CI2CA
TX2P
TX2N
TX1P
TX1N
TX0P
TX0N
TXCP
TXCN
VCC33
R0XCN
R0XCP
R0X0N
R0X0P
R0X1N
R0X1P
R0X2N
R0X2P
CSCL
CSDA
INT
CEC_D
CEC_A
R4PWR5V
DSCL4
DSDA4
R3PWR5V
CBUS_HPD3
DSCL3
DSDA3
R2PWR5V
CBUS_HPD2
DSCL2
DSDA2
SBVCC33
MICOM_VCC33
R1PWR5V
CBUS_HPD1
DSCL1
DSDA1
R0PWR5V
CBUS_HPD0
DSCL0
DSDA0
RSVDL
VCC33_2
R3X2P
R3X2N
R3X1P
R3X1N
R3X0P
R3X0N
R3XCP
R3XCN
R1XCN
R1XCP
R1X0N
R1X0P
R1X1N
R1X1P
R1X2N
R1X2P
VCC33_1
RSVDL_1
R2XCN
R2XCP
R2X0N
R2X0P
R2X1N
R2X1P
R2X2N
R2X2P
HDMI_TX2P
HDMI_TX2N
HDMI_TX1P
HDMI_TX1N
HDMI_TX0P
HDMI_TX0N
HDMI_TXCP
HDMI_TXCN
HDMI_3V3
HDMI0_CLKN
HDMI0_CLKP
HDMI0_RX0N
HDMI0_RX0P
HDMI0_RX1N
HDMI0_RX1P
HDMI0_RX2N
HDMI0_RX2P
HDMI1_CLKN
HDMI1_CLKP
HDMI1_RX0N
HDMI1_RX0P
HDMI1_RX1N
HDMI1_RX1P
HDMI1_RX2N
HDMI1_RX2P
HDMI2_CLKN
HDMI2_CLKP
HDMI2_RX0N
HDMI2_RX0P
HDMI2_RX1N
HDMI2_RX1P
HDMI2_RX2N
HDMI2_RX2P
S33
S34
R542 10R
HDMI0_5V
C924 100n 10V
47k R492
HDMI1_5V
R543 10R
C925 100n 10V
HDMI1_HPDIN
HDMI_0_SCL
HDMI_0_SDA
HDMI_1_SCL
HDMI_1_SDA
SIDE_HDMI_2+
SIDE_HDMI_2-
SIDE_HDMI_1+
SIDE_HDMI_1-
SIDE_HDMI_0+
SIDE_HDMI_0-
SIDE_HDMI_C+
SIDE_HDMI_C-
12V_VCC
24V_VCC
F9 330R
F8 330R
CN32
R815 10R
R816 10R
HDMIC_RX2P
HDMIC_RX2N
HDMIC_RX1P
HDMIC_RX1N
HDMIC_RX0P
HDMIC_RX0N
HDMIC_CLKP
HDMIC_CLKN
HDMIC_SCL
HDMIC_SDA
HDMIC_5V
HDMIC_HPDIN
CEC
CN3
10R R554
10R R555
10R R557
10R R556
10R R560
10R R561
10R R559
10R R562
S49
S47
S48
10R R564
10R R558
47k R774
S46
47k R560
47k R501
1k R186
CN30
HDMI1_RX2P
HDMI1_RX2N
HDMI1_RX1P
HDMI1_RX1N
HDMI1_RX0P
HDMI1_RX0N
HDMI1_CLKP
HDMI1_CLKN
HDMI1_SCL
HDMI1_SDA
HDMI1_5V
HDMI1_HPDIN
CEC
R519 10R
R526 10R
R524 10R
R527 10R
R525 10R
R523 10R
R522 10R
R528 10R
R521 10R
R520 10R
R529 10R
47k R488
47k R485
47k R486
1k R187
CN1
SIDE_HDMI_2+
SIDE_HDMI_2-
SIDE_HDMI_1+
SIDE_HDMI_1-
SIDE_HDMI_0+
SIDE_HDMI_0-
SIDE_HDMI_C+
SIDE_HDMI_C-
SIDE_HDMI_SCL
SIDE_HDMI_SDA
SIDE_HDMI_5V
SIDE_HDMI_HPD
CEC
MHL_POWER
R551 10R
R550 10R
R549 10R
R547 10R
R548 10R
R546 10R
R545 10R
R544 10R
R552 10R
R553 10R
47k R489
47k R497
47k R498
1k R185
MHL_POWER
Q43
FDC642P
5V_VCC
33k R456
R216 47R
33k R455
Q5
BC848B
R33 4k7
3V3_VCC
R34 4k7
MHL_CONTROL
C658 100n 10V
S44
S45
S42
S43
S40
S41
S38
S39
HDMI_TXCP
HDMI_TXCN
HDMI_TX0P
HDMI_TX0N
HDMI_TX1P
HDMI_TX1N
HDMI_TX2P
HDMI_TX2N
HDMI1_CLKP
HDMI1_CLKN
HDMI1_RX0P
HDMI1_RX0N
HDMI1_RX1P
HDMI1_RX1N
HDMI1_RX2P
HDMI1_RX2N
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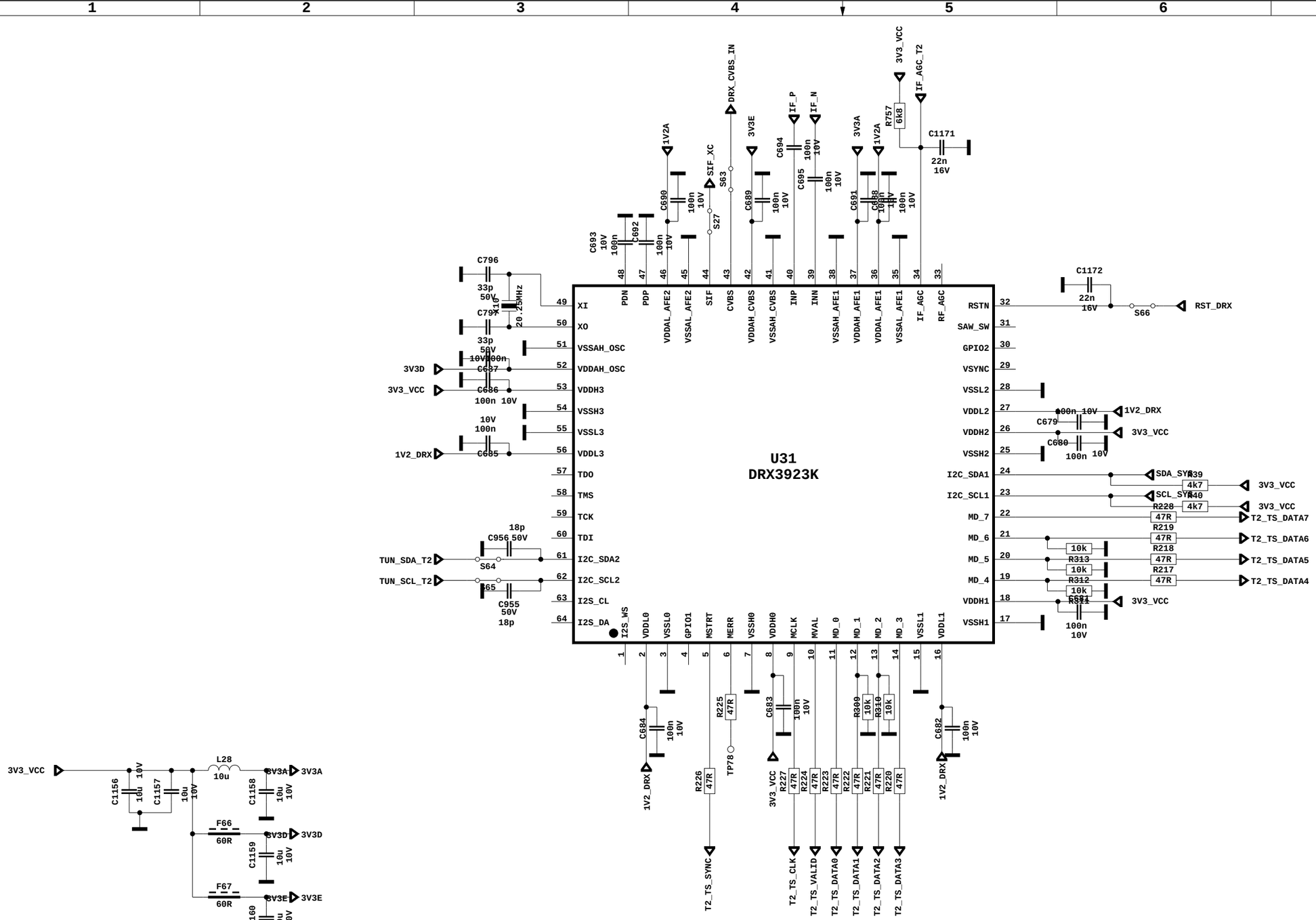
A3
SCH NAME :ALPK_TAMERY
SHEET: OF:
DRAWN BY :15-HDMI
20-10-2010_15:34







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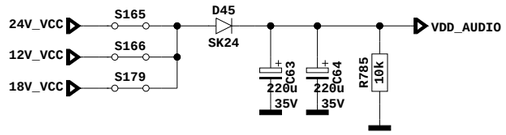
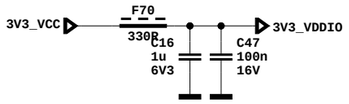
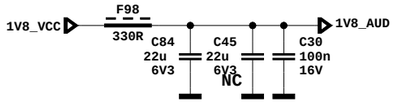
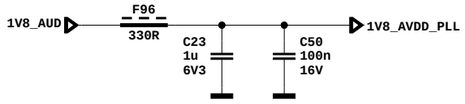
| VESTEL | PROJECT NAME : 17mb65 | A3 |
| SCH NAME : 16-DRXK | SHEET: 17 OF: 16 | |
| DRAWN BY : ALPK-TAMERY | 20-10-2010_19:10 | |

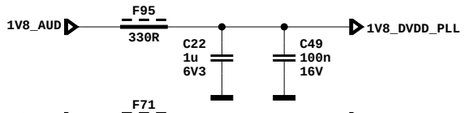


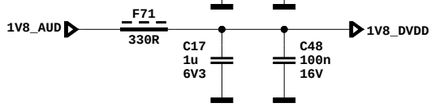



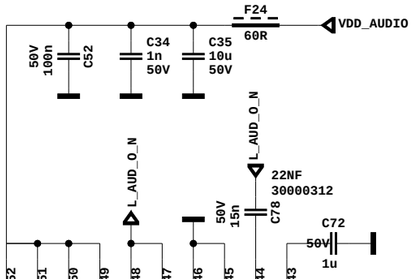



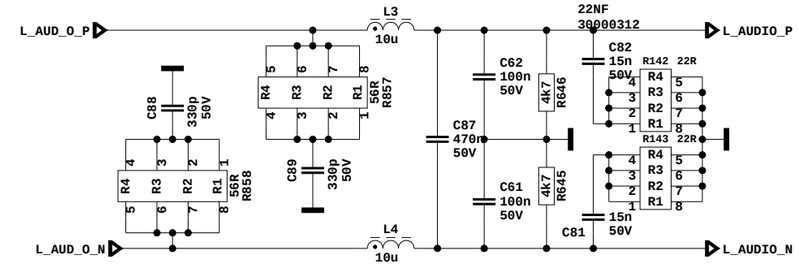



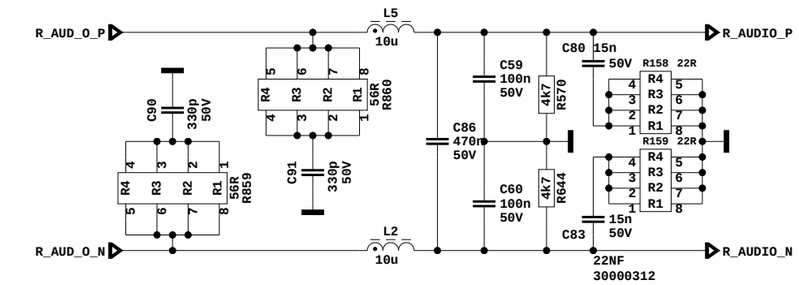

Please Place These Capacitors near pin#12 and pin#13

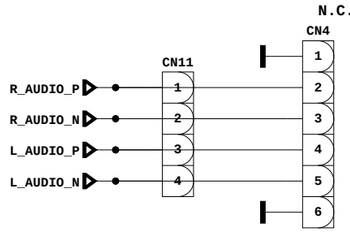


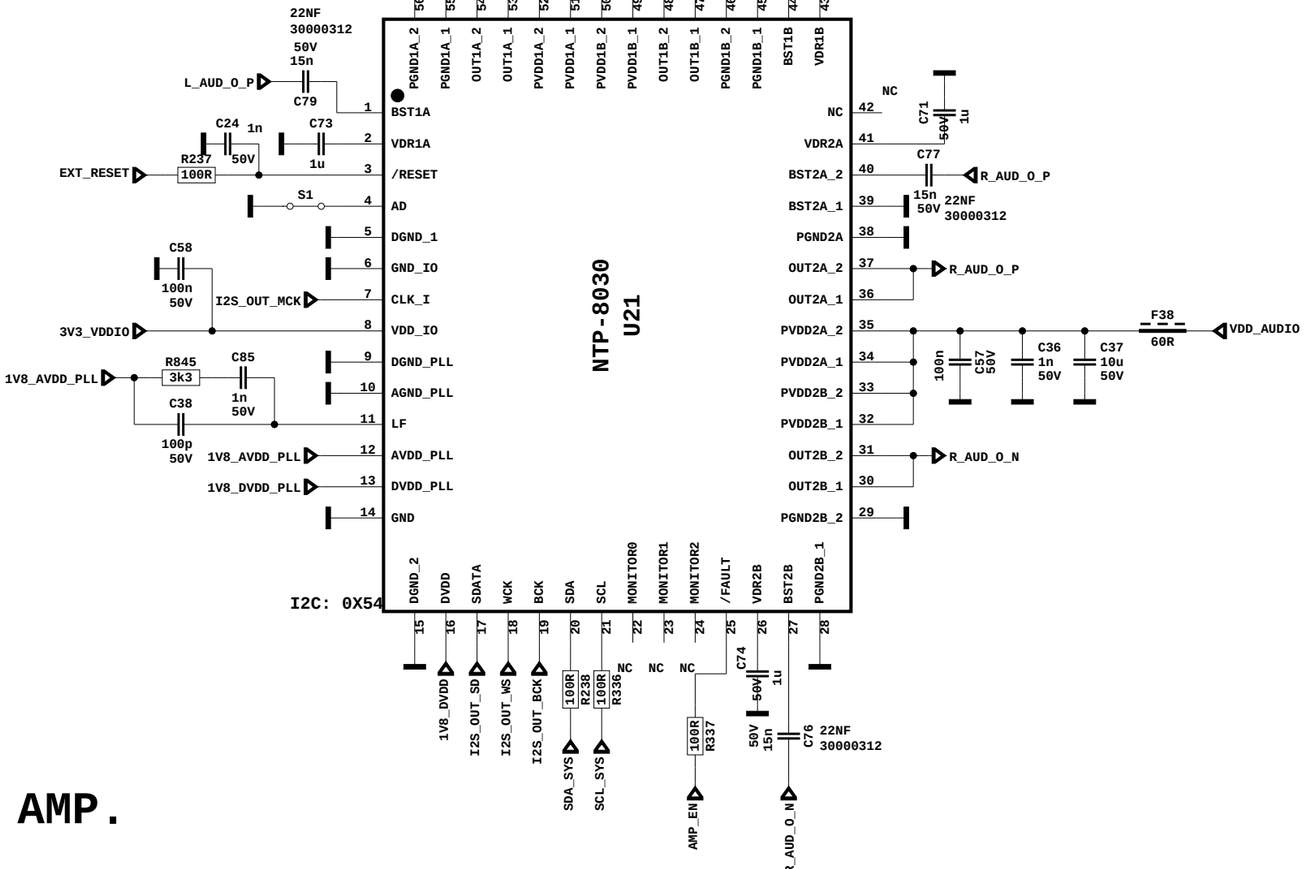



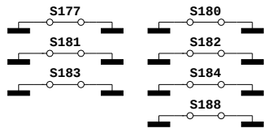




# AUDIO AMP.

| | | |
|---|---|---|
| VESTEL | PROJECT NAME :17mb65 | A3 |
| SCH NAME :18-AUDIO_AMP | | SHEET:18OF:17 |
| DRAWN BY :ALPK/TAMERY | | 04-11-2010_14:49 |